MOHAMMED SATHAK A J COLLEGE OF ENGINEERING
Siruseri IT park, OMR, Chennai - 603103

LESSON PLAN			
Department of ECE			
Name of the Subject	Microprocessors and Microcontrollers	Name of the handling Faculty	M.ASHOKKUMAR
Subject Code	EC8691	Year / Sem	III/V - CSE&IT
Acad Year	2022-2023	Regulation	2017

Course Objectives

Study the Architecture of 8086 microprocessor
Learn the design aspects of I/O and Memory Interfacing circuits.
Study about communication and bus interfacing.
Study the Architecture of 8051 microcontroller

Course Outcomes

Design , implement and execute the programs on 8086 microprocessor
Explain the communication and Bus interfacing
Design I/O and Memory Interfacing circuits.
Design,implement and execute the programs on 8051 microcontroller
Design and implement 8051 microcontroller based systems.

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB /PPT / NPTEL/MOOC/ etc)	Blooms Level (L1-L6)	CO	PO
	UNIT I THE 8086 MICROPROCESSOR						
1	Introduction to 8086 – Microprocessor architecture	T1	1	BB	L2	CO1	PO1-PO3
2	8086 Segment registers	T1	1	BB	L2	CO1	PO1-PO3
3	Addressing Modes	T1	1	PPT	L2	CO1	PO1-PO3
4	Instruction set and assembler directives	T1	1	BB	L2	CO1	PO1-PO3,PO5
5	Assembly language programming	T1	1	BB	L3	CO1	PO1-PO3
6	Modular Programming	T1	1	BB	L2	CO1	PO1-PO3
7	Stacks - Procedures – Macros	T1	1	BB	L2	CO1	PO1-PO3
8	Interrupts and Interrupt service routines	T1	1	BB	L2	CO1	PO1-PO3
9	Byte and String Manipulation	T1	1	BB	L2	CO1	PO1-PO3
Suggested Activity: MCQ							
Evaluation method : MCQ - Google Form							
	UNIT II 8086 SYSTEM BUS STRUCTURE						
10	8086 signals	T1	1	BB	L1	CO2	PO1,PO2
11	System bus timing –System design using 8086	T1	1	PPT	L2	CO2	PO1-PO3
12	System bus timing –System design using 8086	T1	1	BB	L2	CO2	PO1-PO3
13	IO programming	T1	1	PPT	L2	CO2	PO1-PO3
14	Introduction to Multiprogramming	T1	1	BB	L2	CO2	PO1-PO3
15	System Bus Structure	T1	1	BB,PPT	L2	CO2	PO1-PO3
16	Multiprocessor configurations • Coprocessor	T1	1	PPT	L2	CO2	PO1-PO3
17	Closely coupled and loosely Coupled configurations	T1	1	PPT	L2	CO2	PO1-PO3
18	Introduction to advanced processors • The 8087 Numeric Data Processor • The 8089 I/O Processor	T1	1	PPT	L2	CO2	PO1-PO3
Suggested Activity: Inclass activity QUIZ on 8086 signals							
Evaluation method : Based on the students (group) performance marks will be awarded							

UNIT III I/O INTERFACING							
19	Memory Interfacing and I/O interfacing	T1	1	BB	L2	CO3	PO1-PO3
20	Serial and Parallel communication interface	T1	1	BB	L2	CO3	PO1-PO3
21	D/A and A/D Interface	T1	1	BB	L3	CO3	PO1-PO3,PO5
22	Timer:• Architecture• Signal Description • Operating modes• Programming	T1	1	PPT	L3	CO3	PO1-PO3
23	Keyboard /display controller	T1	1	PPT	L3	CO3	PO1-PO3
24	Interrupt controller	T1	1	BB	L2	CO3	PO1-PO3
25	DMA controller	T1	1	BB,PPT	L2	CO3	PO1-PO3
26	Case studies: • Traffic Light control • LED display	R1,T1	1	BB,PPT	L4	CO3	PO1-PO3,PO4
27	Programming and applications Case studies • Keyboard display interface	R1,T1	1	PPT	L4	CO3	PO1-PO3,PO5
Suggested Activity: Case studies							
Evaluation method : Case studies report							
UNIT IV MICROCONTROLLER							
28	Architecture of 8051	T2	1	PPT	L2	CO4	PO1-PO3
29	Register set	T2	1	PPT	L1	CO4	PO1-PO3
30	Special Function Registers (SFRs)	T2	1	PPT	L2	CO4	PO1-PO3
31	I/O Pins Ports and Circuits	T2	1	BB	L2	CO4	PO1-PO3
32	Instruction set Data transfer and Arithmetic Instructions	T2	1	BB	L2	CO4	PO1-PO3
33	Jump, Loop and Call Instructions	T2	1	BB	L2	CO4	PO1-PO3
34	Addressing modes	T2	1	BB	L2	CO4	PO1-PO3
35	Assembly language programming	T2	1	PPT	L3	CO4	PO1-PO3
36	Assembly language programming	T2	1	BB	L3	CO4	PO1-PO3
Suggested Activity: Seminar on Applications of microcontroller- Group Presentation							
Evaluation method : Based on presentation marks will be awarded							
UNIT V INTERFACING MICROCONTROLLER							
37	Programming 8051 Timers	T2	1	BB	L2	CO5	PO1-PO3
38	Serial Port Programming • Basics of Serial Communication • 8051 Connection to RS232 • 8051 Serial Port Programming in Assembly • Programming the Second Serial Port	T2	1	PPT	L2	CO5	PO1-PO3
39	Interrupts Programming • 8051 Interrupts • Programming Timer Interrupts • Programming External Hardware Interrupts • Programming the serial Communication Interrupt	T2	1	PPT	L2	CO5	PO1-PO3
40	LCD & Keyboard Interfacing	T2	1	PPT	L3	CO5	PO1-PO3,PO12
41	Keyboard Interfacing	T2	1	PPT	L3	CO5	PO1-PO3
42	ADC & DAC interfacing	T2	1	PPT	L3	CO5	PO1-PO3,PO12
43	Sensor Interfacing	T2	1	PPT	L3	CO5	PO1-PO3
44	External Memory Interface	T2	1	PPT	L2	CO5	PO1-PO3
45	Stepper Motor and Waveform generation	T2	1	PPT	L3	CO5	PO1-PO3
Suggested Activity: Mini project Using 8051.(Group)							
Evaluation method : Based on implementation mark will be awarded							

Content Beyond the Syllabus Planned	
1	An Insight on ARM , PIC controller
2	Design of Microcontroller based system using PROTEUS (Keyboard Interface)
	Text Books
1	Yu-Cheng Liu, Glenn A.Gibson, "Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design", Second Edition, Prentice Hall of India, 2007.
2	Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", Second Edition, Pearson Education, 2011.
	Reference Books
1	Doughlas V.Hall, "Microprocessors and Interfacing, Programming and Hardware", TMH,2012
	Website / URL References
1	https://nptel.ac.in/courses/106/108/106108100/
2	https://nptel.ac.in/courses/106/108/106108100/
3	https://nptel.ac.in/content/storage2/courses/106108100/pdf/Teacher_Slides/mod3/M3L8.pdf

Blooms Level					
Level 1 (L1) : Remembering	Lower Order Thinking	Fixed Hour Exams	**Level 4 (L4) : Analysing**		Higher Order Thinking
Level 2 (L2) : Understanding			**Level 5 (L5) : Evaluating**		
Level 3 (L3) : Applying			**Level 6 (L6) : Creating**		

Mapping syllabus with Bloom's Taxonomy LOT and HOT										
Unit No	**Unit Name**	**L1**	**L2**	**L3**	**L4**	**L5**	**L6**	LOT	HOT	**Total**
Unit 1	THE 8086 MICROPROCESSOR	0	8	1	0	0	0	9	0	9
Unit 2	8086 SYSTEM BUS STRUCTURE	1	8	0	0	0	0	9	0	9
Unit 3	I/O INTERFACING	0	4	3	2	0	0	7	2	9
Unit 4	MICROCONTROLLER	1	6	2	0	0	0	9	0	9
Unit 5	INTERFACING MICROCONTROLLER	0	4	5	0	0	0	9	0	9
Total		2	30	11	2	0	0	43	2	45
Total Percentage		4.44	66.67	24.44	4.44	0.00	0.00	95.56	4.44	100

CO PO Mapping

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	3	2	2	-	-	-	-	-	-	-	-	-	0	0
CO2	3	2	2	-	1			-	-	-	-	-	0	0
CO3	3	2	2	-	-	-	-	-	-	-	-	-	0	0
CO4	3	2	2	-	-	-	-	-	-	-	-	1	1	0
CO5	3	2	2	-	-	-	-	-	-	-	-	-	1	0
Avg	3	2	2	0	1	0	0	0	0	0	0	1	1	0

Justification for CO-PO mapping	
CO1	Design and implement programs on 8086 microprocessor requires a fundamental knowledge in mathematics and engineering funadamentals (PO1) and an analytical approach to digital Logic circuits (PO2).It requires an understanding of design concepts (PO3)
CO2	Understand the functionality of 8086 system bus requires fundamental knowledge in mathematics and engineering funadamentals (PO1), and a strong analytical approach (PO2).It requires an understanding of design concepts (PO3).
CO3	Design I/O circuits requires fundamental knowledge in mathematics and engineering funadamentals (PO1), and a strong analytical approach to design an I/O circuits (PO2). It requires depth of knowledge in the design concepts (PO3). Implementation of applications using kits(PO5)
CO4	Design Memory Interfacing circuits requires fundamental knowledge in mathematics and engineering funadamentals(PO1), and a strong analytical approach to design a Memory Interfacing circuits (PO2).It requires depth of knowledge in the design concepts (PO3).
CO5	Design and implement 8051 microcontroller based systems requires fundamental knowledge in mathematics and engineering funadamentals (PO1), and a medium analytical approach (PO2).It requires an understanding of design concepts and tools(PO3).Less use of design tools(PO5)

3	**High level**	**2**	**Moderate level**	**1**	Low level

Name & Sign of Faculty Incharge :

Name & Sign of Subject Expert :

Head of the Department :

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