MOHAMMED SATHAK A J COLLEGE OF ENGINEERING

Siruseri IT park, OMR, Chennai - 603103

LESSON PLAN

Department of Electronics and Communication Engineering

Name of the Subject	DIGITAL SYSTEM DESIGN	Regulation	2021
Subject Code	EC3352	Year / Sem	II/III
Academic Year	2022-2023	Batch	2021-2025

Course Objective

To introduce Fundamental of digital circuits - postulates,Theoems and simplification methods.

To Practice the formal design procedures for the analysis and design of combinational circuits

To Analyse the formal design procedures for the analysis and design of Synchronous and Asynchronous Sequential circuits

To learn Integrated Logic Families

To learn about Semiconductor Memories and to Study about Implementation of PLDS

Course Outcome

At the end of the course, the students should be able to:

CO1: Apply different methods used for simplification of Boolean functions

CO2:Design and implement Various Combinational digital circuits.

CO3:Analyse and Design Various Synchronous and Asynchronous Sequential circuits

CO4:Ability to Understand Integrated Logic Families

CO5: Ability to Understand Semiconductor Memories and Analyse PLDS

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB / PPT / NPTEL / MOOC / etc)	Blooms Level (L1-L6)	CO	PO
	UNIT I BASIC CONCEPTS						
1	Recview of Number Systems & Representation	T1	**1**	BB	L1	CO1	PO1-PO2,PO12
2	Conversion -Problems	T1	**1**	BB	L2	CO1	PO1-PO2
3	Review of Boolean Algebra and Theorems (lab)	TI	**1**	BB,NPTEL	L1	CO1	PO1-PO3
4	Sum of Product and Product of Sum Simplification	T1	**1**	BB	L2	CO1	PO1-PO3
5	Canonical Forms,Minterm and Maxterms	T1	**1**	BB	L2	CO1	PO1-PO3
6	Simplification of Boolean Expression -K Map	T1	**1**	BB	L3	CO1	PO1-PO3
7	K-Mapcompletely Specified Problems	T1	**1**	BB	L3	CO1	PO1-PO3,PO12
8	K-Map Incompletely Specified Problems	T1,R1	**1**	BB,PPT	L3	CO1	PO1-PO3
9	Implementations of Boolean Expression Using Universal Gates (lab)	T1	**1**	BB,PPT	L2	CO1	PO1-PO3
10	Implementation Problems (lab)	T1	**1**	BB	L3	CO1	PO1-PO3
11	Tabulation Method	T1	**1**	BB	L3	CO1	PO1-PO3
12	Problems-Tabulation Method	R1	**1**	BB	L3	CO1	PO1-PO3
13	Revision-Lab Session						

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any **Tutorial & Quiz** : Implementation - kmap,quine Mc cluskey method (Tutorial/Quiz)

Evaluation method : Report

	UNIT II COMBINATIONAL LOGIC CIRCUITS						
14	Problems Formulation and Design of Combinational Circuits	T1	**1**	Lab Demo	L2	CO2	PO1-PO3,PO5
15	Code Converters (xs-3,BCD,Binary,Gray)	T1	**1**	Lab Demo	L3	CO2	PO1-PO3
16	Code converter -Continuation (Lab)	R1	**1**	Lab Demo	L3	CO2	PO1-PO3
17	Half and Full Adders (lab)	T1	**1**	Lab Demo	L2	CO2	PO1-PO3
18	Binary Parallel Adder (lab)	R1	**1**	BB	L2	CO2	PO1-PO3,
19	CarryLook Ahead Adder	R1	**1**	BB	L2	CO2	PO1-PO3
20	BCD Adder	T1	**1**	BB,NPTEL	L2	CO2	PO1-PO3
21	Magnitude Comparator (lab)	R1	**2**	Lab Demo	L3	CO2	PO1-PO3
25	Decoder & Encoder (lab)	T1	**1+2**	Lab Demo	L2	CO2	PO1-PO3
26	Priority Encoder,Problems in Decoder & Encoder Design	T1	**1**	Lab Demo	L4	CO2	PO1-PO3
27	Mux And Demultiplexer	T1	**1**	Lab Demo	L4	CO2	PO1-PO3
28	Case Study Review: Digital Tranceiver,7 segment Display Decoder	T1	**1**	case Study	L3	CO2	PO1-PO3,PO12

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any **Mini Project : Design a Seven Segment Display Circuit**

Evaluation method : Designed circuit verified by Demo

	UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS							
29	Latches,Flip Flops,SR FF ,JK FF	T1	1	BB,PPT	L2	CO3	PO1-PO3	
30	T-FF ,D - FF ,Master Slave FF	T1	1	BB,PPT	L2	CO3	PO1-PO3	
31	Triggering of FF,FF Conversion	T1	1	BB	L2	CO3	PO1-PO3	
32	Analysis of Clocked Sequential Circuit	T1	1	BB,PPT	L3	CO3	PO1-PO3	
33	Design of Clocked Sequential Circuits -Moore Model	T1,R3	1	BB	L3	CO3	PO1-PO3,PO4,PO5	
34	Design of Clocked Sequential Circuits -Mealy Model	T1	1	BB	L3	CO3	PO1-PO3,PO5,PO12	
35	State Mnimization & State Assignment	T1,R3	1	BB	L3	CO3	PO1-PO3,PO4,PO5	
36	Lock out Condition and Circuit Implementation	T1	1	BB	L2	CO3	PO1-PO3,PO5,PO12	
40	Counters,Ripple Couter ,Ring Counter (lab)	T1	1+3	BB	L2	CO3	PO1-PO3	
44	Counters Design Problems (Lab)	T1	1+3	BB	L3	CO3	PO1-PO3	
47	Shift Registers ,Universal Shift Registers (Lab)	T1	1+2	BB	L2	CO3	PO1-PO3	
48	Model Developemet overview (Display and Real time Clock)	T1,R3	1	BB	L4	CO3	PO1-PO3,PO4,PO5	
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any							**Miniproject: Design of Rolling Display**	
Evaluation method : Simulation Model /kit								
	UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS							
49	Stable and Unstable States	T1	1	BB	L2	CO3	PO1-PO3,PO12	
50	output Specifications	T1	1	BB	L2	CO3	PO1-PO3	
51	Cycles and Races	T1	1	BB,PPT	L2	CO3	PO1-PO3	
52	State Reduction	T1,R1	1	PPT	L3	CO3	PO1-PO3,PO4	
53	State Reduction- Continuation	T1	1	PPT	L3	CO3	PO1-PO3,PO4	
54	Race Free Assignments	T1	1	BB	L2	CO3	PO1-PO3,PO4,PO5,PO12	
55	Hazards and Essential Hazards	T1,R3	1	BB	L2	CO3	PO1-PO3	
56	Design free Hazard Free Circuits	T1	1	BB	L3	CO3	PO1-PO3,PO4	
57	Fundamental Mode Sequential Circuits	T1	1	BB	L3	CO3	PO1-PO3	
58	Problems-Fundamental Mode	T1	1	BB	L3	CO3	PO1-PO3	
59	Pulsed Mode Sequential Circuits	T1	1	BB	L3	CO3	PO1-PO3	
60	Problems-Pulsed Mode	T1,R3	1	BB	L3	CO3	PO1-PO3	
61	Lab Session		6					
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any							**Quiz: Sequential Circuits**	
Evaluation method : Online MCQ Quiz								
	UNIT V LOGIC FAMILIES & PROGRAMMABLE LOGIC DEVICES							
67	Logic Families and Propagation Delay	T1,R1	1	BB	L2	CO4	PO1-PO3,PO4	
68	Fan -In ,Fan-Out ,Noise Margin	T1	1	BB	L2	CO4	PO1-PO3	
69	RTL,TTL	T1,R1	1	BB	L2	CO4	PO1-PO3	
70	ECL,CMOS,Comparison of Logic Families	T1	1	BB	L2	CO4	PO1-PO3	
71	Implementation of Combinational Logic (lab)	T1	1+3	BB	L3	CO5	PO1-PO3	
74	Implementation of Sequential logic -PROM,PLA	T1,R1	1	BB	L3	CO5	PO1-PO3	
75	PAL-Design	T1,R1	1	BB	L3	CO5	PO1-PO3	
76	Basic Memory-Staic ROM	T1	1	BB	L3	CO5	PO1-PO3,PO4,PO5	
77	Problems in Designing PROM,PLA	T1	1	BB	L3	CO5	PO1-PO3	
78	Problems in Designing PAL	T1	1	BB	L3	CO5	PO1-P03	
79	PROM,EPROM	T1	1	BB	L2	CO5	PO1-PO3	
80	EEPROM,EAPROM	T1	1	BB	L2	CO5	PO1-PO3,PO4,PO5	
83	Lab Session		3					
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any							**deign a 4 bit adder/subtractor circuit using verilog HDL**	
Evaluation method: Simulate the program								
Content Beyond the Syllabus Planned								
1	Introduction to VLSI							
2	Recent technology in VLSI							

Text Books	
1	M. Morris Mano and Michael D. Ciletti, 'Digital Design', Pearson, 5th Edition, 2013.(Unit - I -V)
Reference Books	
1	Charles H. Roth, Jr, 'Fundamentals of Logic Design', Jaico Books, 4th Edition, 2002.
2	William I. Fletcher, "An Engineering Approach to Digital Design", Prentice- Hall of India, 1980.
3	Floyd T.L., "Digital Fundamentals", Charles E. Merril publishing company,1982.
4	John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 4 th Edition,2007.
Website / URL References	
1	https://nptel.ac.in/courses/117/106/117106086/
2	https://www.tutorialspoint.com/digital_circuits/digital_circuits_quine_mccluskey_tabular_method.htm
3	https://www.tutorialspoint.com/digital_circuits/digital_circuits_conversion_of_flip_flops.htm
4	https://www.digimat.in/nptel/courses/video/108105132/L01.html
5	https://nptel.ac.in/courses/117/106/117106086/

Blooms Level

Level 1 (L1) : Remembering	Lower Order Thinking	Fixed Hour Exams	Level 4 (L4) : Analysing		Higher Order Thinking	Projects / Mini Projects
Level 2 (L2) : Understanding			Level 5 (L5) : Evaluating			
Level 3 (L3) : Applying			Level 6 (L6) : Creating			

Mapping syllabus with Bloom's Taxonomy LOT and HOT

Unit No	Unit Name	L1	L2	L3	L4	L5	L6	LOT	HOT	Total
Unit 1	BASIC CONCEPTS	2	4	6	0	0	0	12	0	12
Unit 2	COMBINATIONAL LOGIC CIRCUITS	0	6	4	2	0	0	10	2	12
Unit 3	SYNCHRONOUS SEQUENTIAL CIRCUITS	0	6	5	1	0	0	11	1	12
Unit 4	ASYNCHRONOUS SEQUENTIAL CIRCUITS	0	5	7	0	0	0	12	0	12
Unit 5	LOGIC FAMILIES AND PROGRAMMABLE LOGIC DEVICES	0	6	6	0	0	0	12	0	12
Total		2	28	29	3	0	0	0	3	60
Total Percentage		3.33	46.67	48.33	5.00	0.00	0.00	0.00	5.00	100.00

CO PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3	1	1	1	0	0	0	0	0	1	2	0	1
CO2	3	3	2	2	2	1	0	0	0	0	0	2	1	0	2
CO3	3	3	2	1	2	1	0	0	0	0	0	2	2	1	2
CO4	3	2	3	1	2	1	0	0	0	0	0	1	2	1	2
CO5	3	3	2	1	2	0	0	0	0	0	0	2	2	1	2
Avg	3	2.8	2.4	1.2	1.8	0.8	0	0	0	0	0	1.6	1.8	0.6	2

Justification for CO-PO mapping

CO1	Strong correlation for PO1,PO2,PO3 and Less correlation for PO4 is given as the CO1 can be used to apply knowledge of engineering to Identify , formulate ,design and solve the problems.Limited use of modern techniques and design tools PO5 ,less impact on society (PO6),Simulated design tools and integrated chip idea is needed to indulge life long learning persistent learning PO12. An overall impact of electronic circuits design using logic ICs is high PSO1.Adapt to emerge and develop innovation solutions PSO3
CO2	High correlation for PO1,PO2, Medium correlation PO3, is given as the CO2 can be used to apply knowledge of engineering to design and provide solutions and by using relevant simulated tools medium correlation for PO$,PO5/.Medium correlation for PSO1 is given as combinational circuits are required to design and development .Simulated design tools and design idea is needed to indulge in persistent learning PO12. develop Innovative Solutions for Existing ProblemsPSO3
CO3	High correlation for PO1,PO2, Medium correlation PO3, is given as the CO3 can be used to apply knowledge of engineering to Identify , formulate and provide solutions and medium correlation for PO4,PO5 provide solutions by using relevant simulated tools.Medium correlation for PSO1 is given as combinational circuits are required to design and development . Simulated design tools and design idea is needed to indulge in persistent learning PO12.Adapt to emerge and develop innovation solutions PSO3
CO4	High correlation for PO1,PO3, Medium correlation PO2, is given as the CO4 can be used to apply knowledge of engineering to Identify , formulate and provide solutions and Less correlation for PO4,PO5 provide solutions by using relevant simulated tools.Medium correlation for PSO1 is given as combinational circuits are required to design and development Life long .Learning is required on Integrated Logic Families.PO12.Emerging technologies develope innovative ideas.PSO3
CO5	High correlation for PO1,PO2, Medium correlation PO3, is given as the CO5 can be used to apply knowledge of engineering to Identify , formulate and provide solutions and Less correlation for PO4, PO5 provide solutions by using relevant simulated tools.Medium correlation for PSO1 is given as combinational circuits are required to design and development .Simulated design tools and design idea is needed to indulge in persistent learning PO12Learning is required on Integrated Semiconductor memories .PO12.Adapt to emerge and develop innovation solutions in PLDs -PSO3

3	High level	2	Moderate level	1	Low level

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