VLSI DESIGN

UNIT I : INTRODUCTION TO MOS TRANSISTOR

INTRODUCTION TO MOS TRANSISTOR

- MOS Transistor, Long-Channel I-V Charterstics, C-V Charterstics, Non ideal I-V Effects,
- CMOS logic, Inverter, DC Transfer characteristics
- Pass Transistor, Transmission gate,
- Layout Design Rules, Gate Layouts, Stick Diagrams,
- RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.

transistor

- A transistor is a device that presents a
- ➢ high input resistance to the signal source, drawing little input power, and
- ➢ a low resistance to the output circuit, capable of supplying a large current to drive the circuit load.

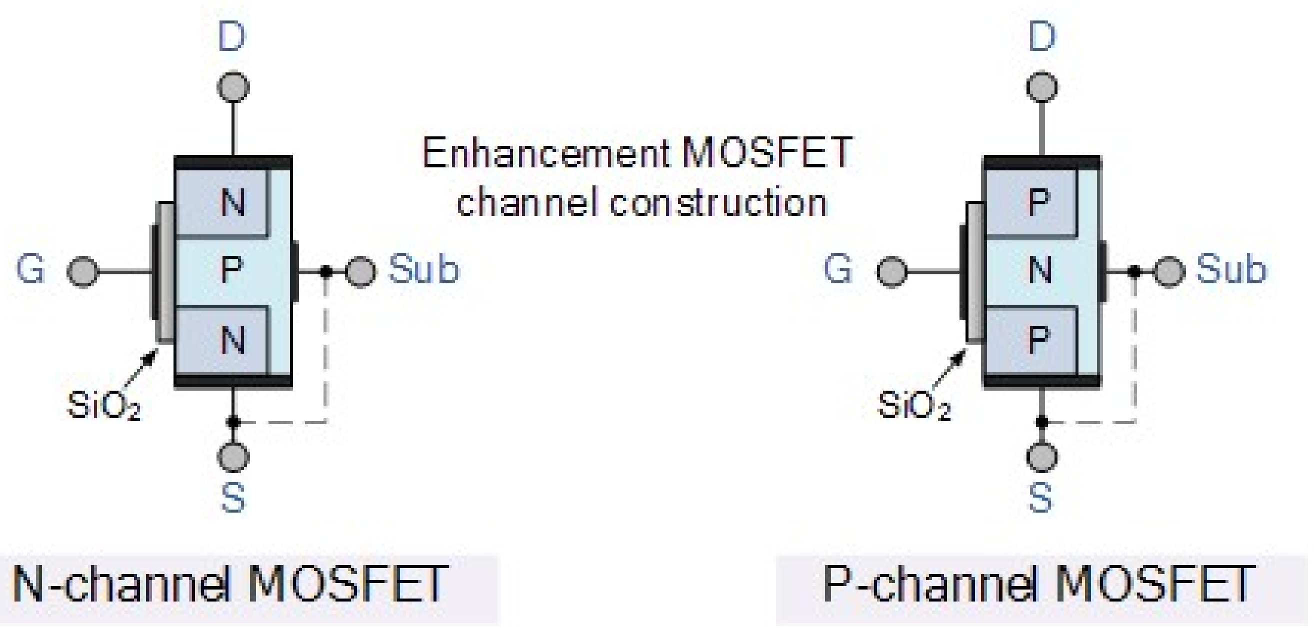
field-effect transistor or FET

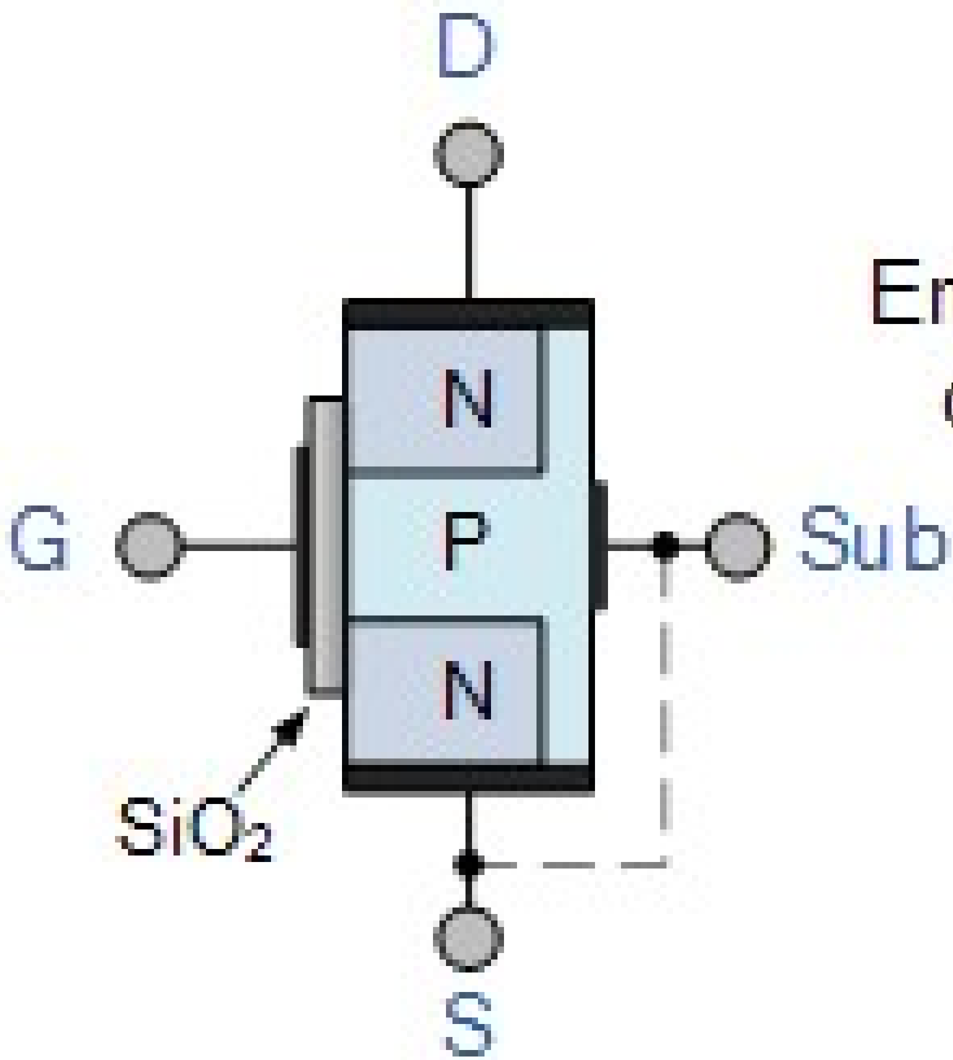
field-effect transistor or FET refers to

- the gate turns the transistor (inversion layer) on and off with an electric field through the oxide.

Metal Oxide Semiconductor FET

- two PN junctions
- four terminal device – Source, Gate, Drain, substrate/body
- majority-carrier device

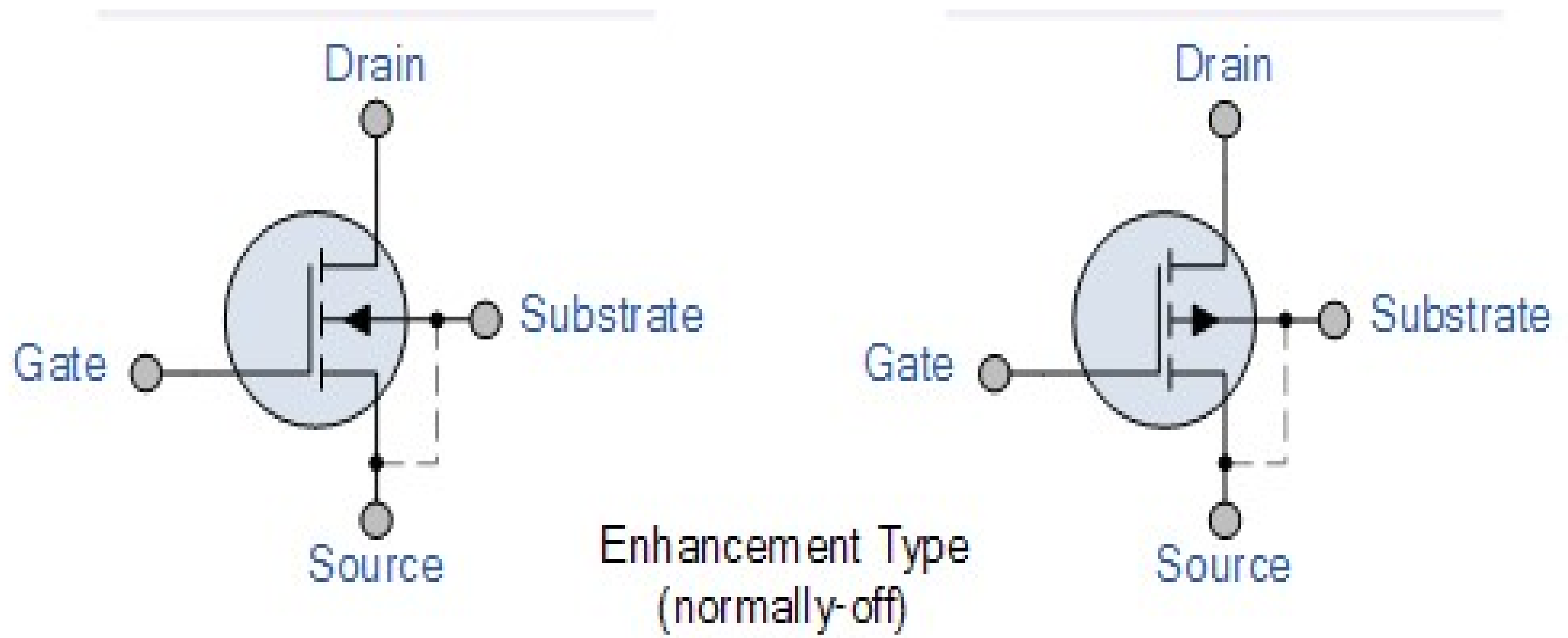




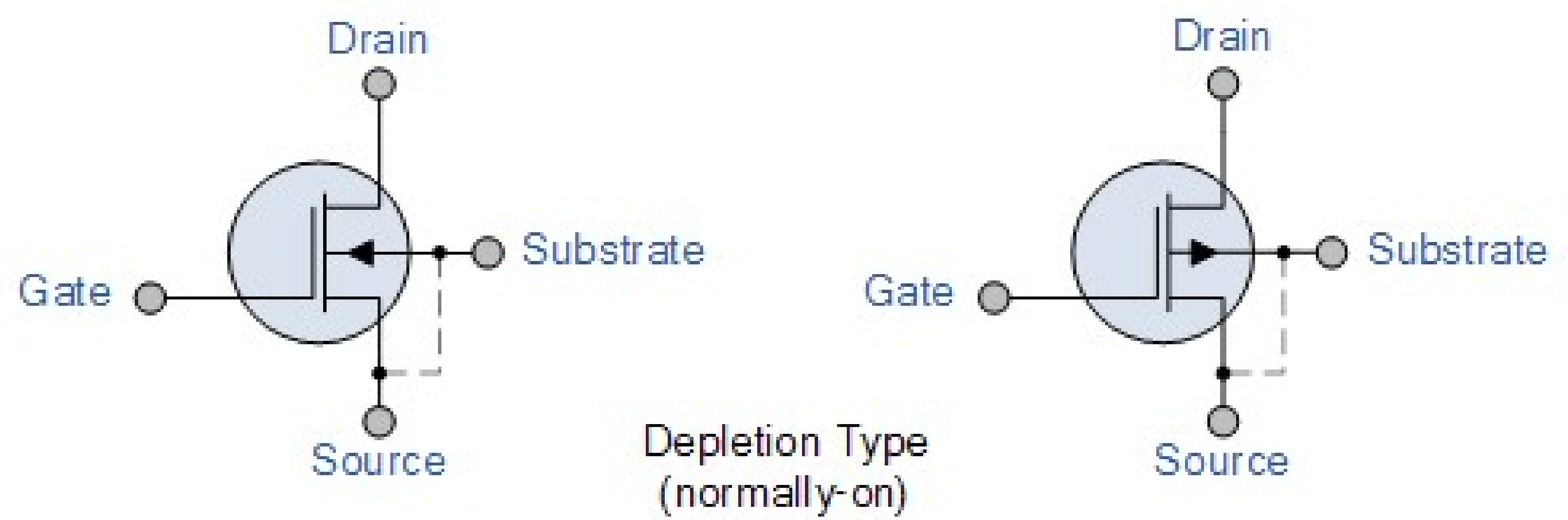
N-channel MOSFET

Enhancement MO
channel constru

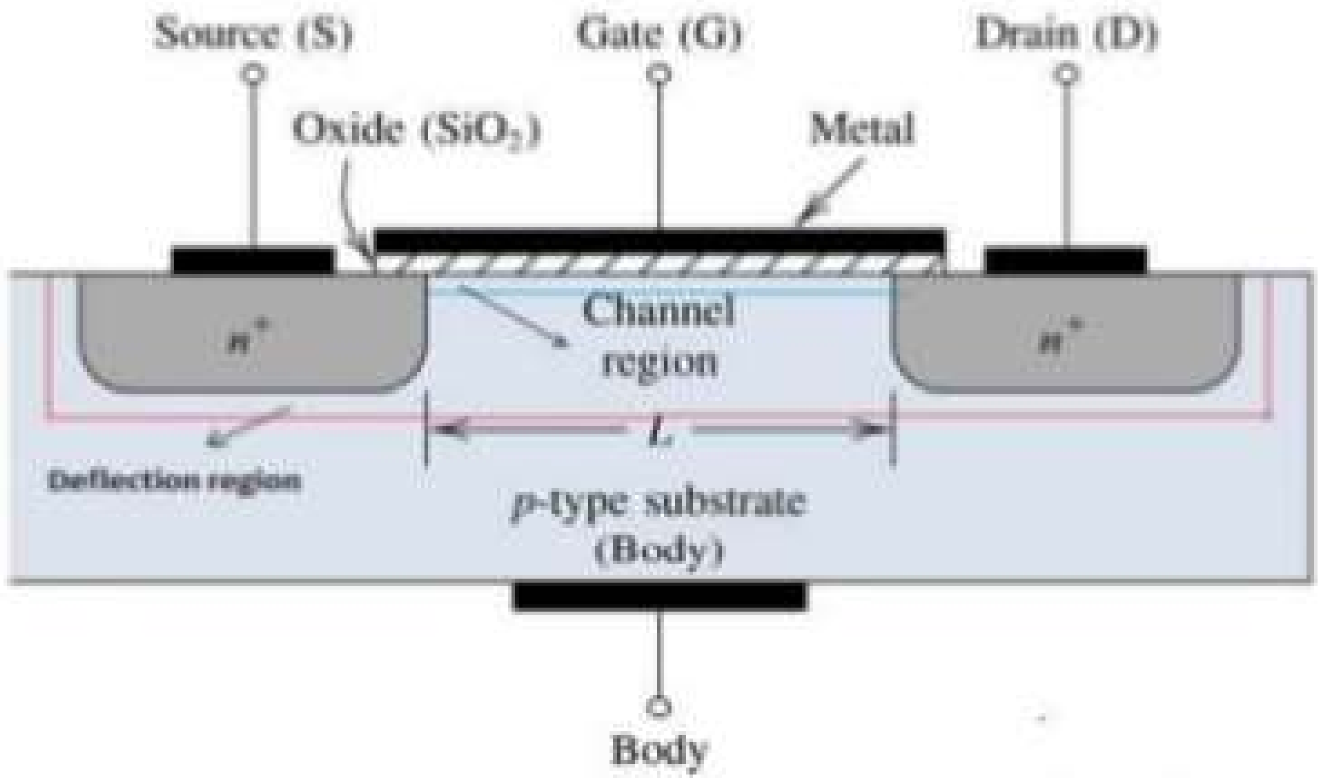
- Enhancement Type – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.



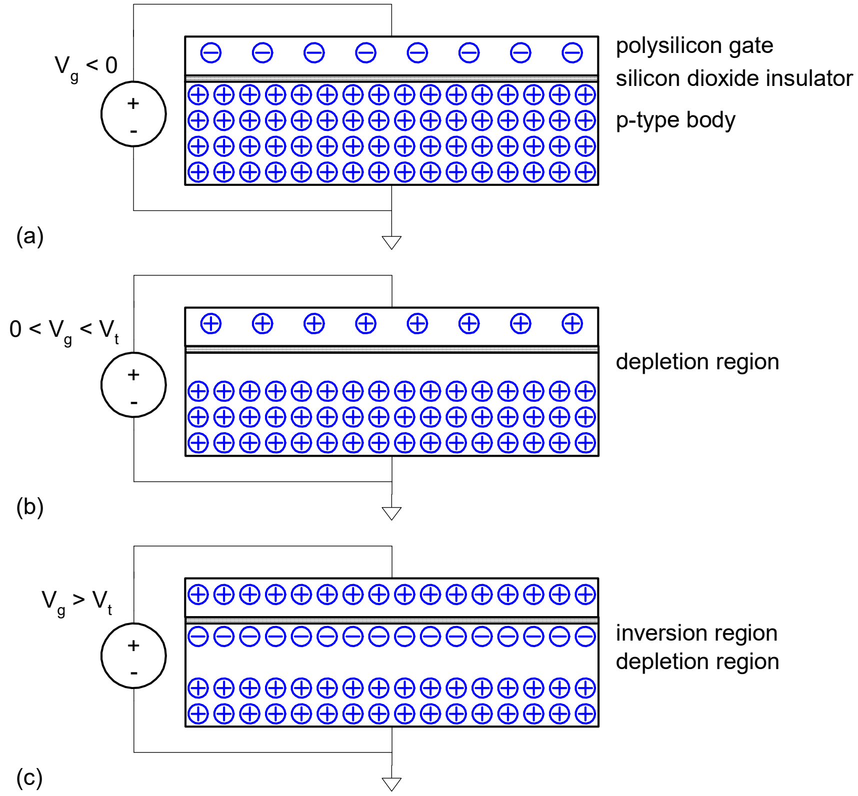
- Depletion Type – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.



N Channel Enhancement MOSFET

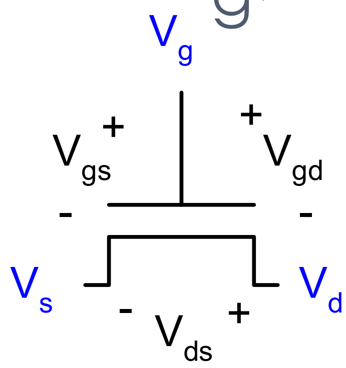


Operating modes
Accumulation, Depletion, Inversion



Terminal Voltages

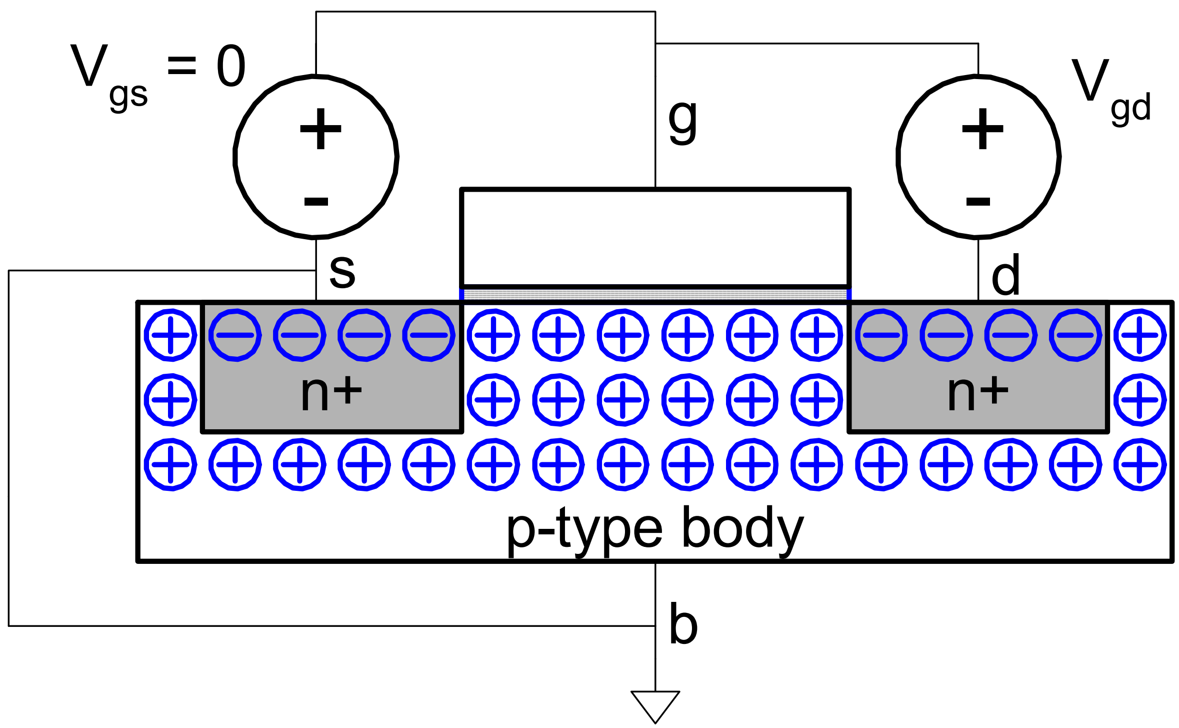
- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$



- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*

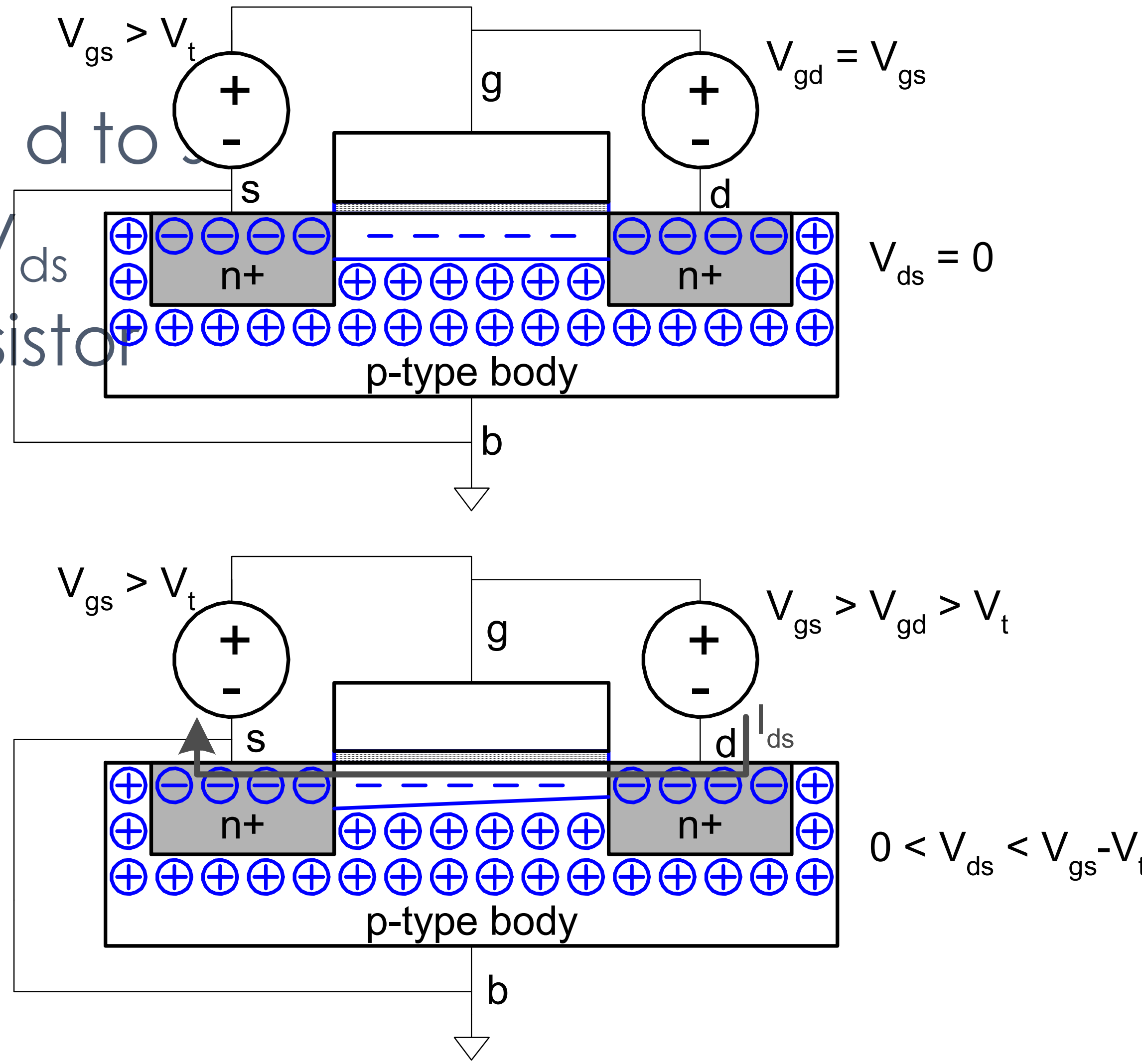
nMOS Cutoff

- No channel
- $I_{ds} = 0$



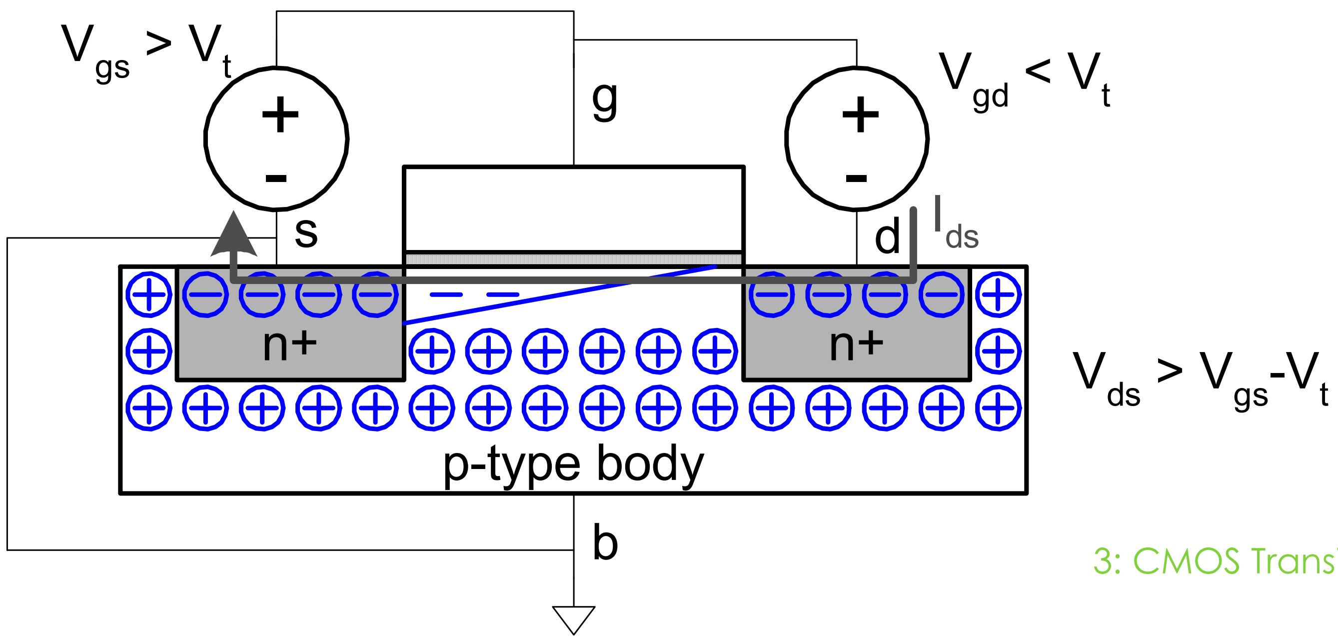
nMOS Linear

- Channel forms
- e^- from s to d
- Current flows from d to s
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source

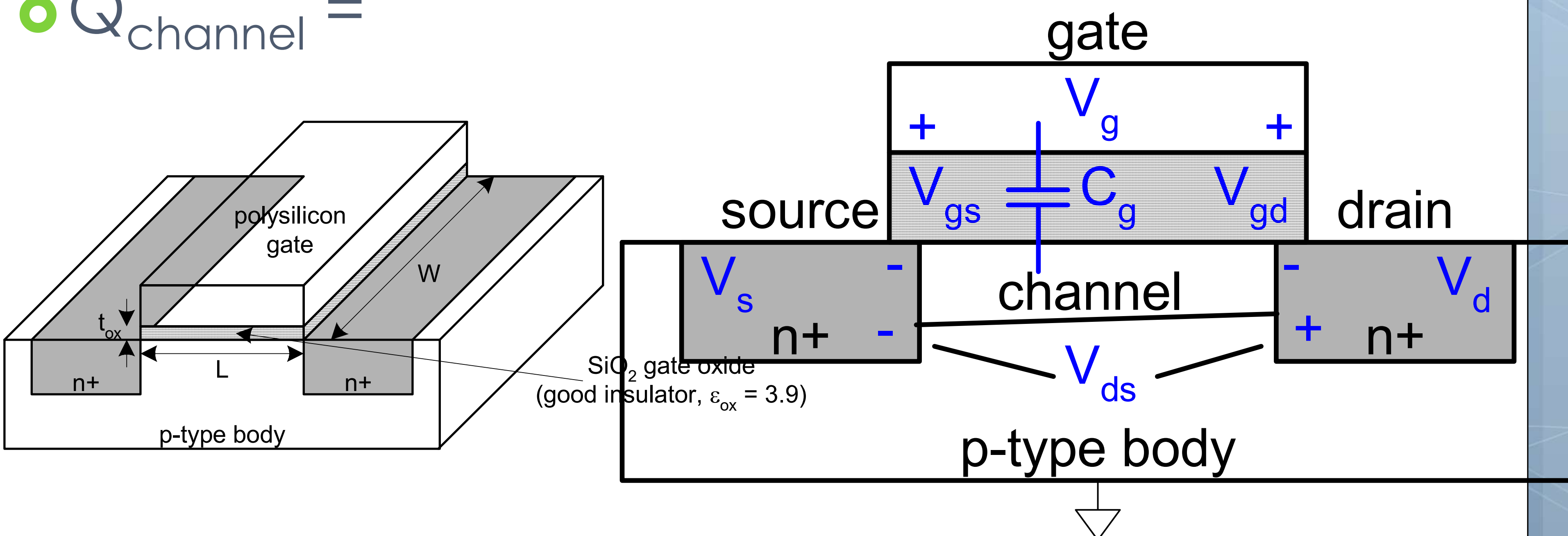


I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

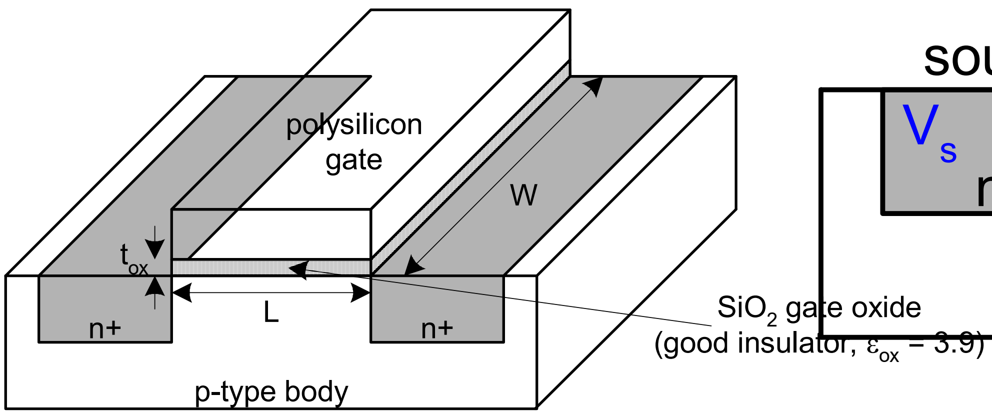
Channel Charge

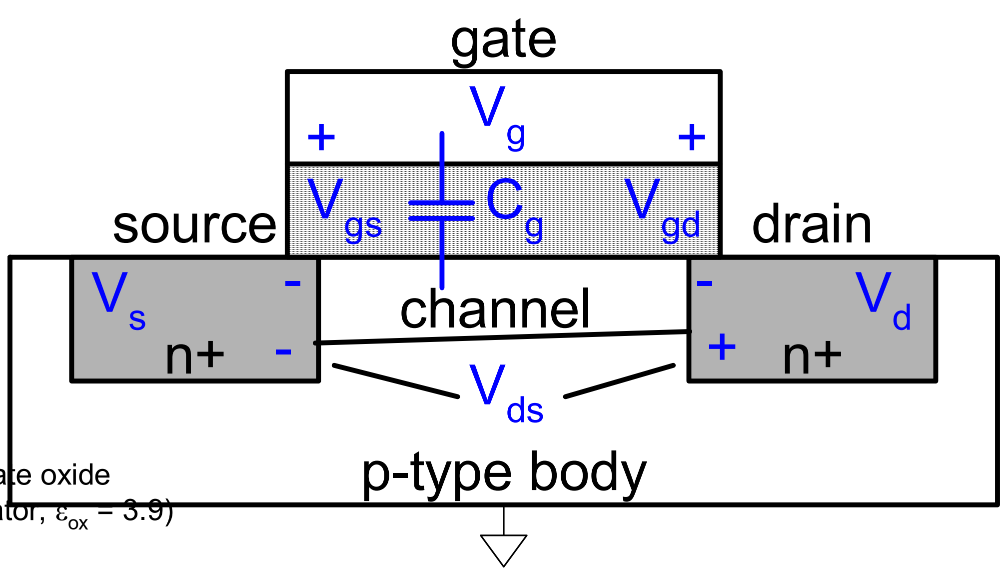
- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel}$ =



Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- C =

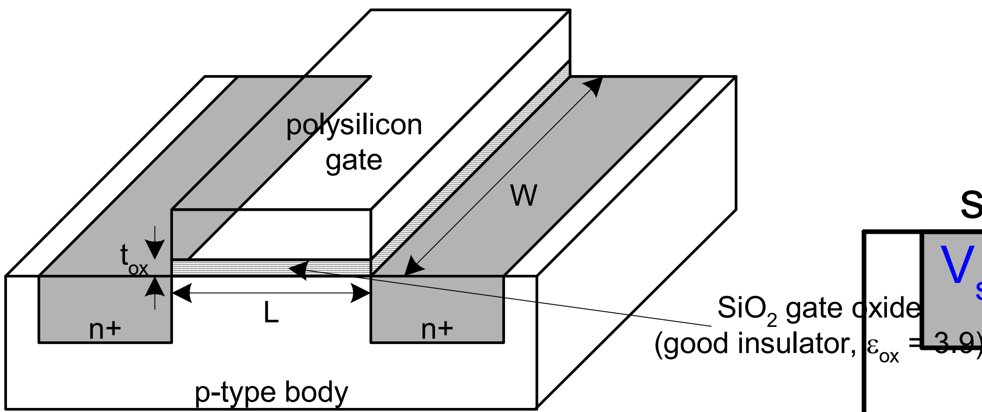


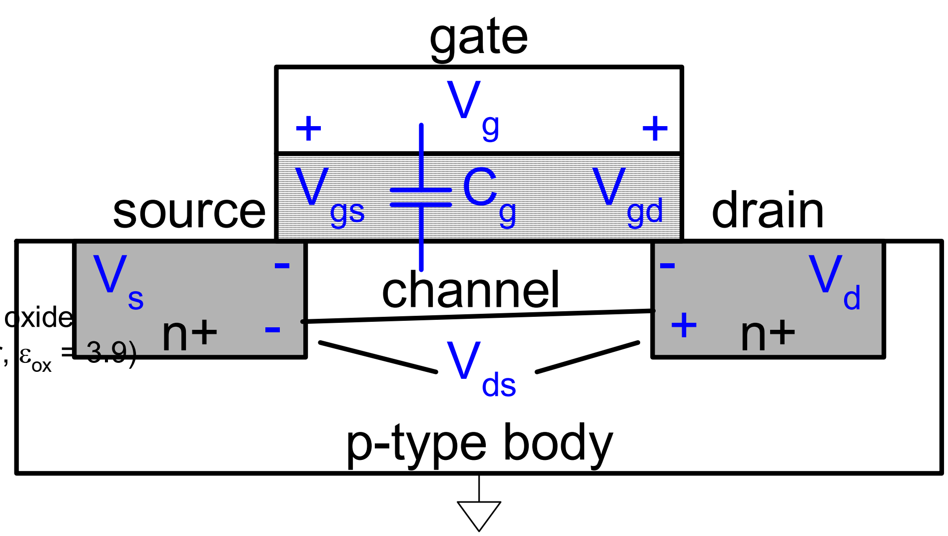


Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$
- V =

$$C_{ox} = \varepsilon_{ox} / t_{ox}$$

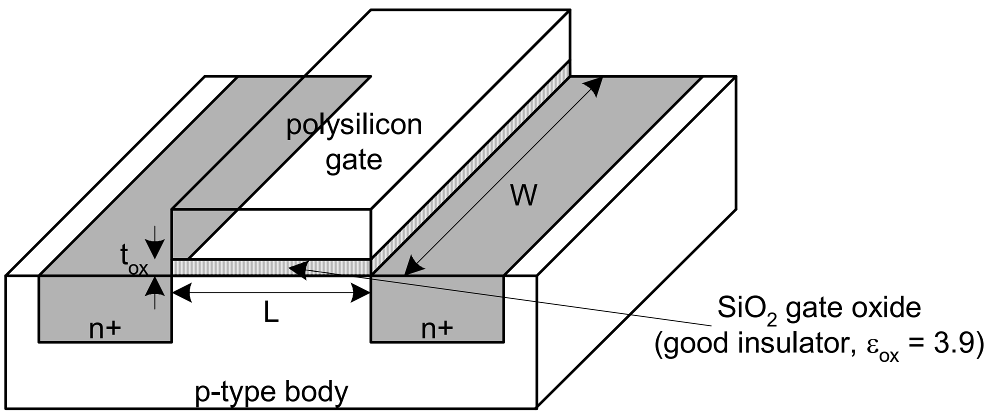


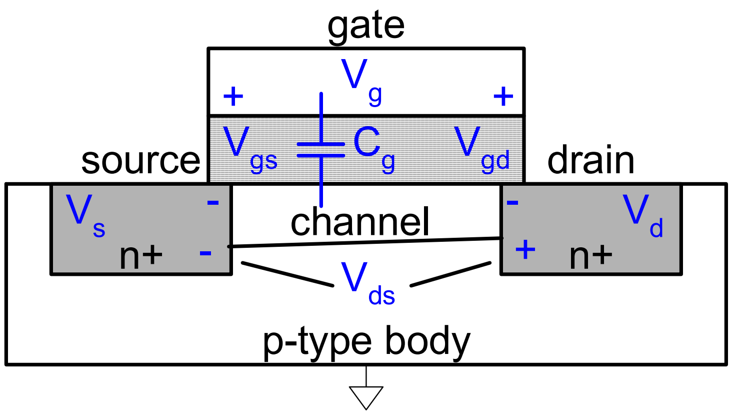


Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$
- $Q = Cox\ WL^{*}\ (V_{gs} - V_{ds}/2) - V_t$

$$C_{ox} = \varepsilon_{ox} / t_{ox}$$





Carrier velocity

- Charge is carried by e-
- Carrier velocity v proportional to lateral E-field between source and drain
- v =

Carrier velocity

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- $v = \mu E$ μ called mobility
- E =

Carrier velocity

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- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t =$

Carrier velocity

- Charge is carried by e-
- Carrier velocity v proportional to lateral E-field between source and drain
- $v = \mu E = \mu V_{ds}/L$
- μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$
  - $Time, t = L/ \mu V_{ds} * L = L*L/ \mu V_{ds}$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} =$$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time t each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$=$$

  - = Cox WL * [(Vgs – Vds/2) –Vt]µVds/ L*L

nMOS Linear I-V

- Now we know
  - How much charge Q_{channel} is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} =$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - {V_{dsat}}/{2}\right)V_{dsat}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current
- Ids= β [Vgs-Vt –(Vgs-Vt)/2] (Vgs-Vt)
- = β[(Vgs-Vt/2)] (Vgs-Vt)
- = β/2 [Vgs-Vt]

$I_{ds} =$

$=$

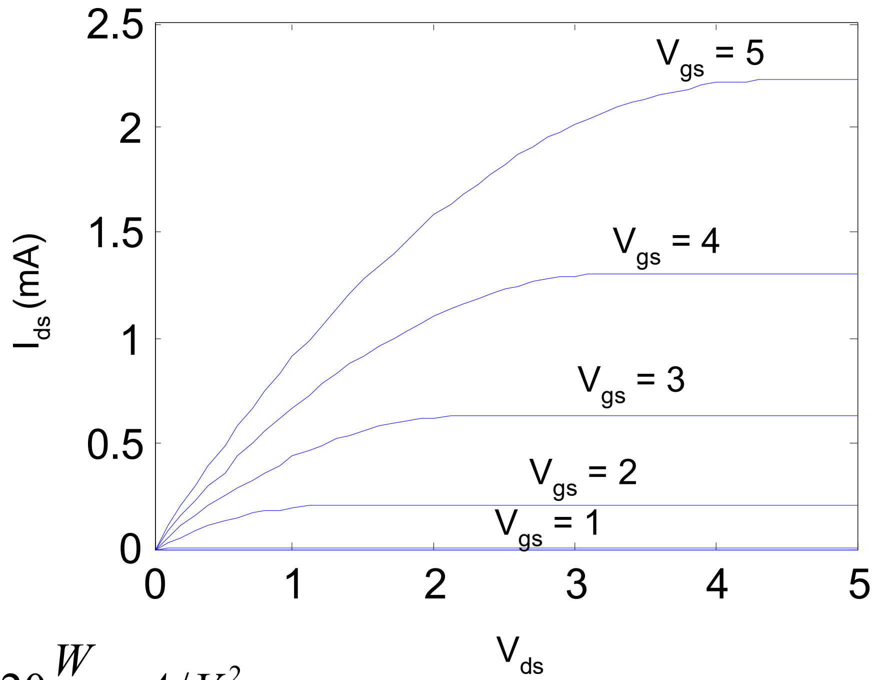
nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

Example

- 0.6 μm process (Example)
  - From AMI Semiconductor
  - t_{ox} = 100 Å
  - μ = 350 cm²/V*s
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\mu A/V^2$$

pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V{*}s$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

Non-ideal Transistor I-V effects

- Non ideal transistor Behavior
  - Channel Length Modulation
  - Threshold voltage effects
    - Body effect
    - Drain induced Barrier Lowering (DIBL)
    - Short Channel effects
  - High Field Effects
    - Mobility Degradation
    - Velocity Saturation
  - Leakage
    - Sub threshold Leakage
    - Gate Leakage
    - Junction Leakage
  - Process and Environmental Variations

Ideal Transistor I-V

- Schockley long channel transistor model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \ \& \ V_{gs} \geq V_t & \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \ \& \ V_{gs} \geq V_t & \text{saturation} \end{cases}$$

$$\beta = \mu \frac{\varepsilon ox}{tox} \frac{W}{L}$$

Ideal vs. Simulated nMOS I-V plots

- 65 nm IBM process, VDD=1.0V

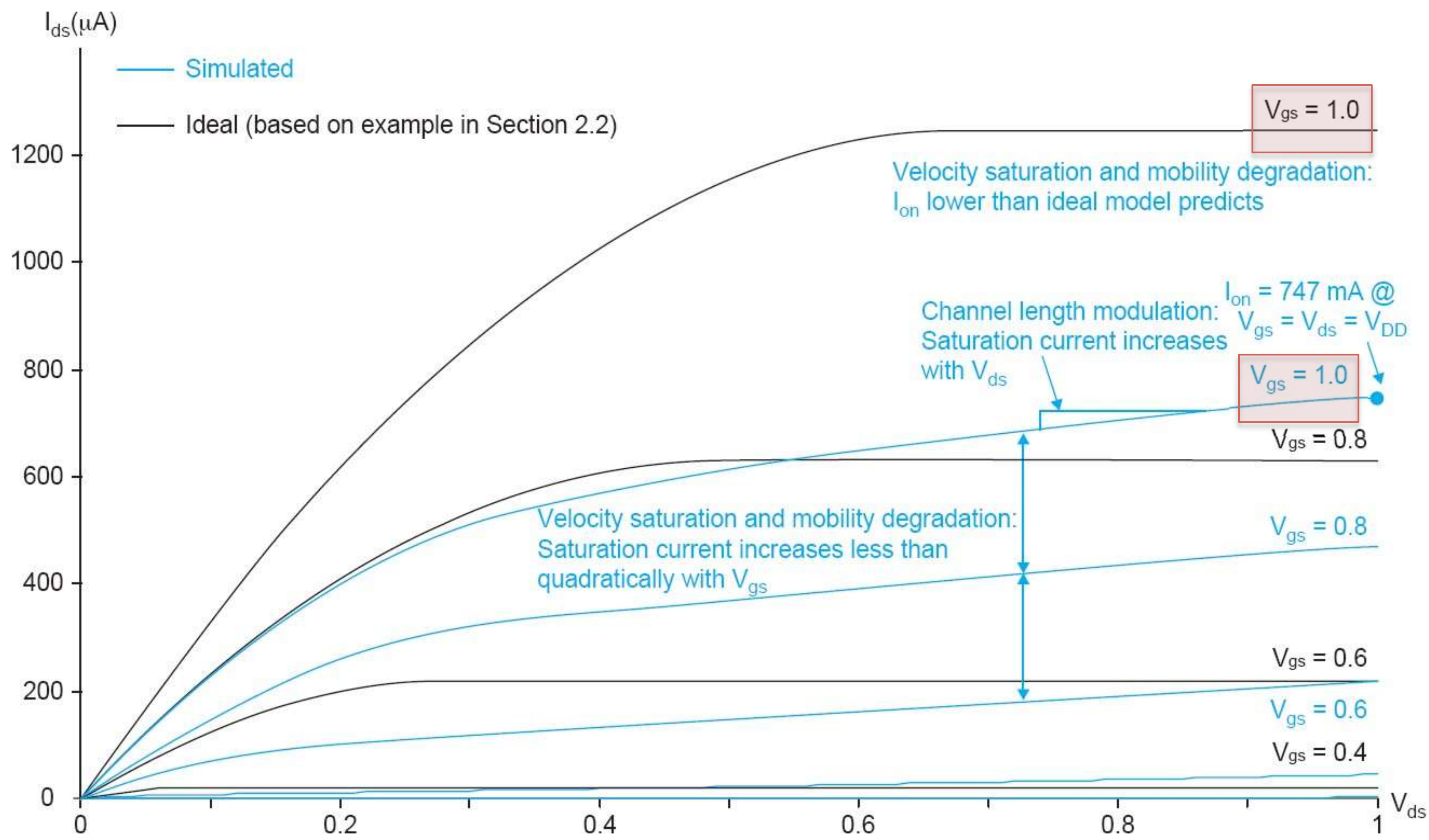
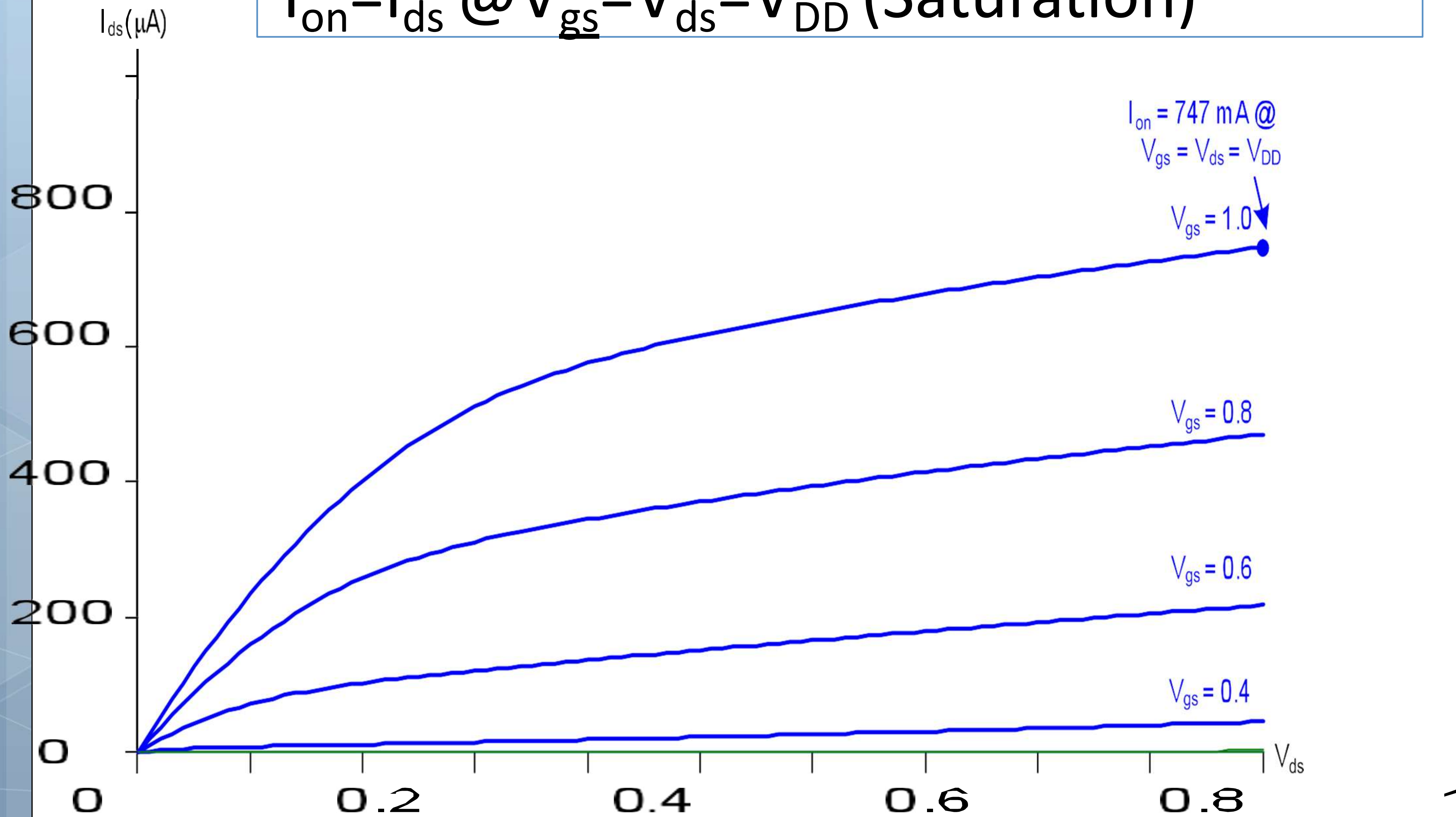


FIGURE 2.14 Simulated and ideal I-V characteristics

ON and OFF Current (1/3)

$I_{on}=I_{ds}$ @$V_{gs}=V_{ds}=V_{DD}$ (Saturation)



ON and OFF Current (2/3)

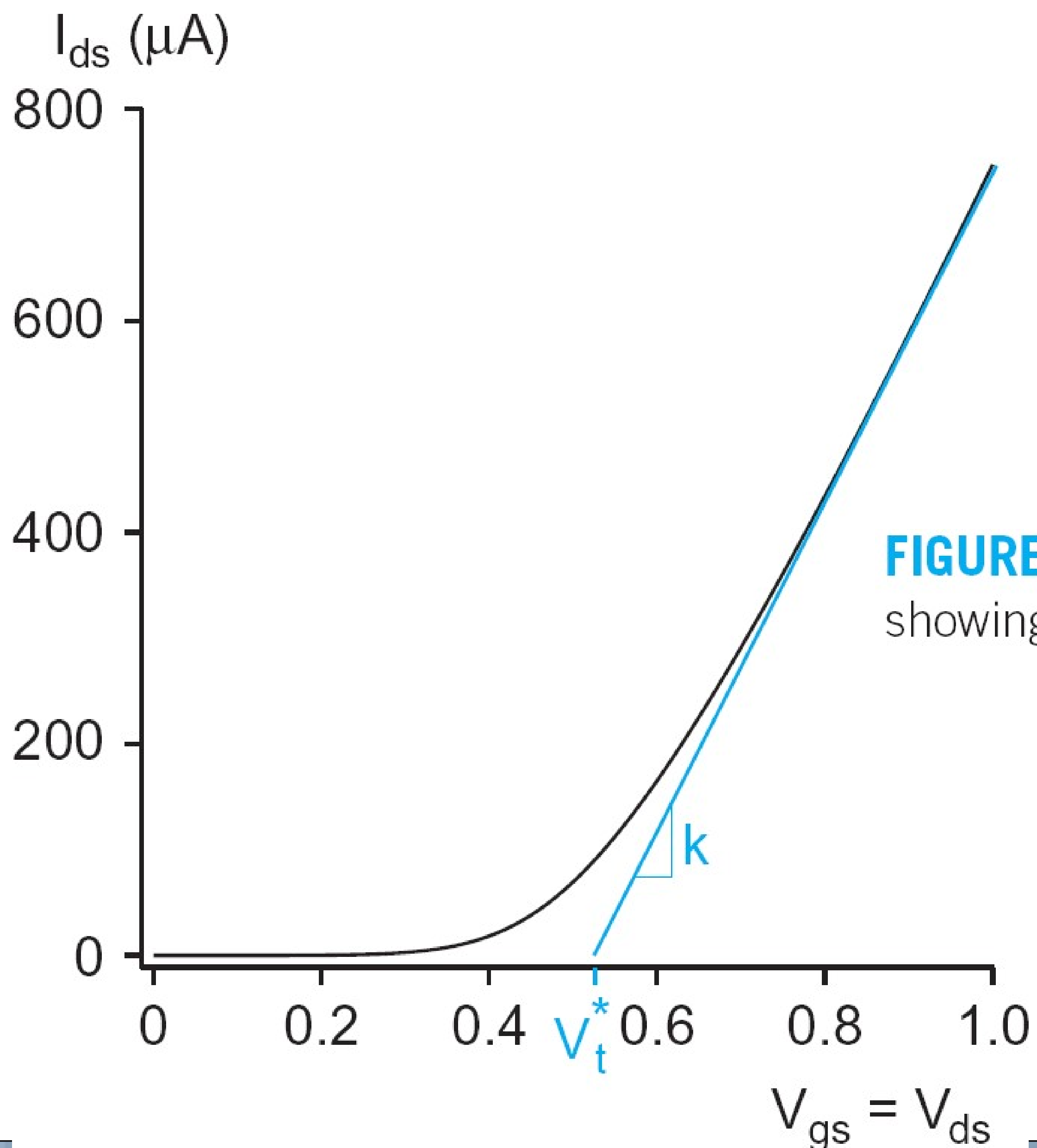
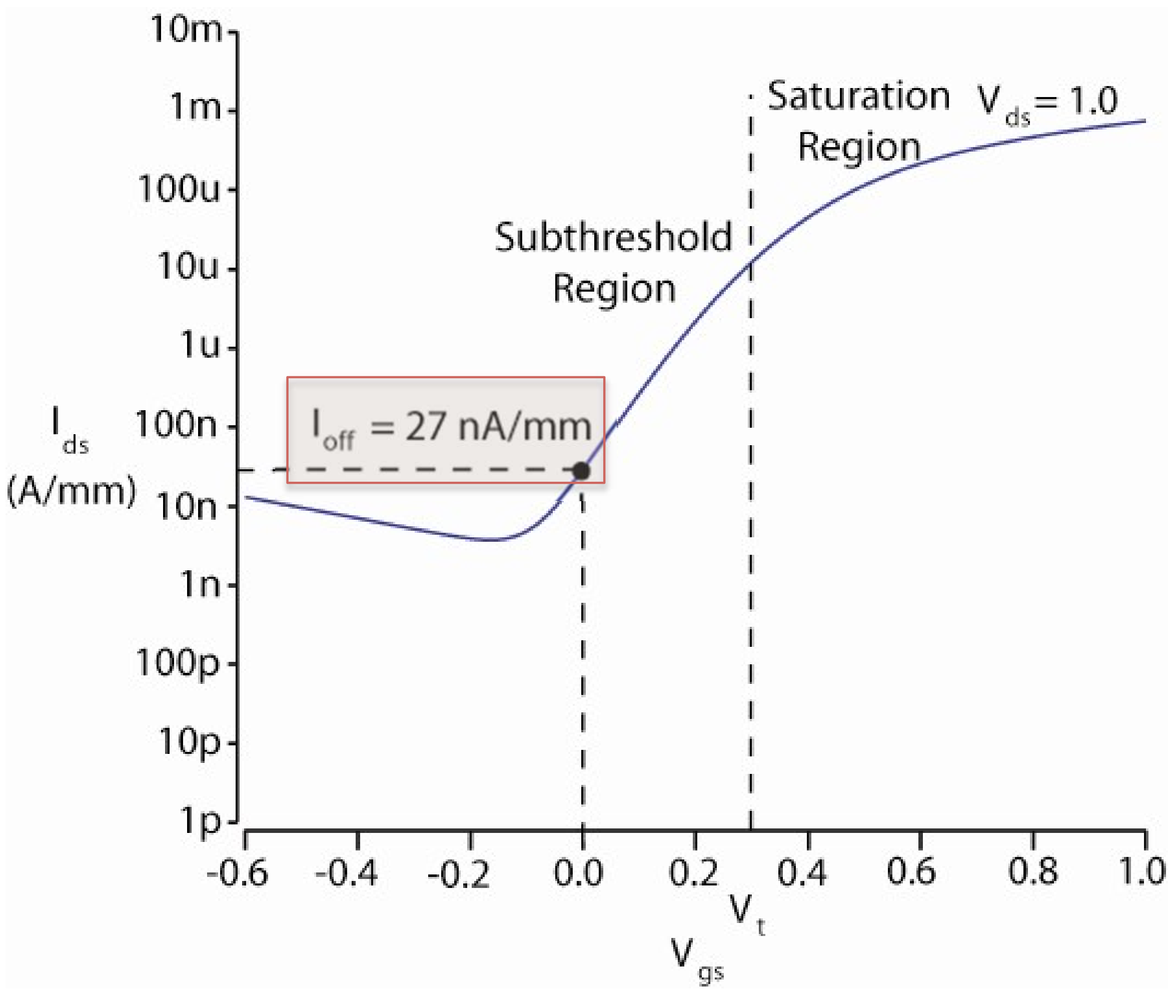


FIGURE 2.17 I_{ds} vs. V_{gs} in saturation, showing good linear fit at high V_{gs}

ON and OFF Current (3/3)

$I_{off}=I_{ds}$ @$V_{gs}=0$, $V_{ds}=V_{DD}$ (Cutoff)



Channel Length Modulation

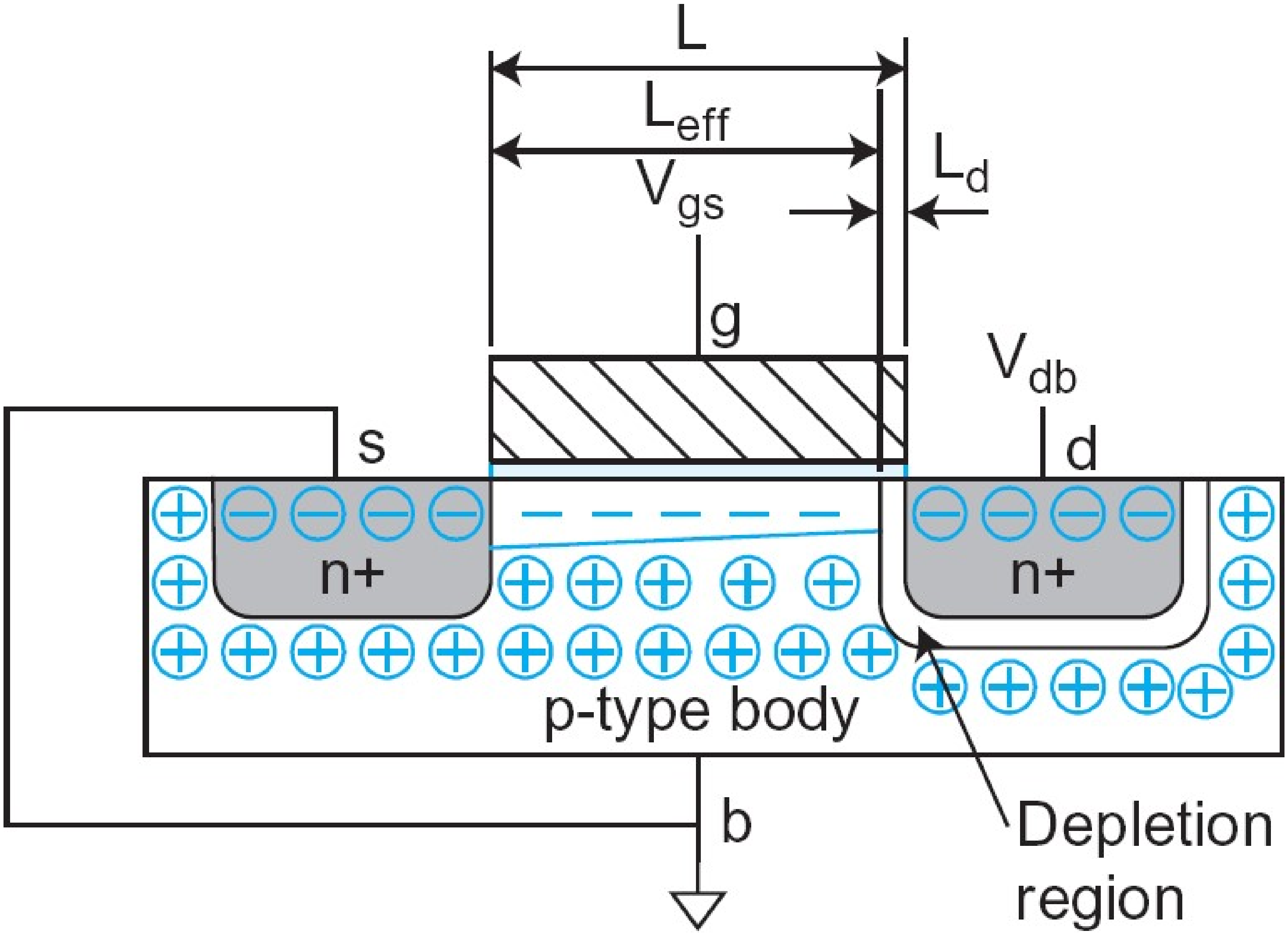
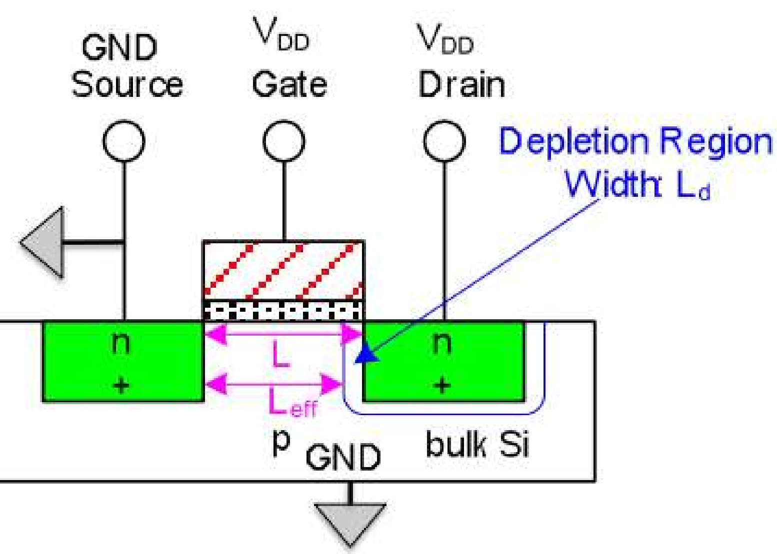


FIGURE 2.18 Depletion region shortens effective channel length

Channel Length Modulation

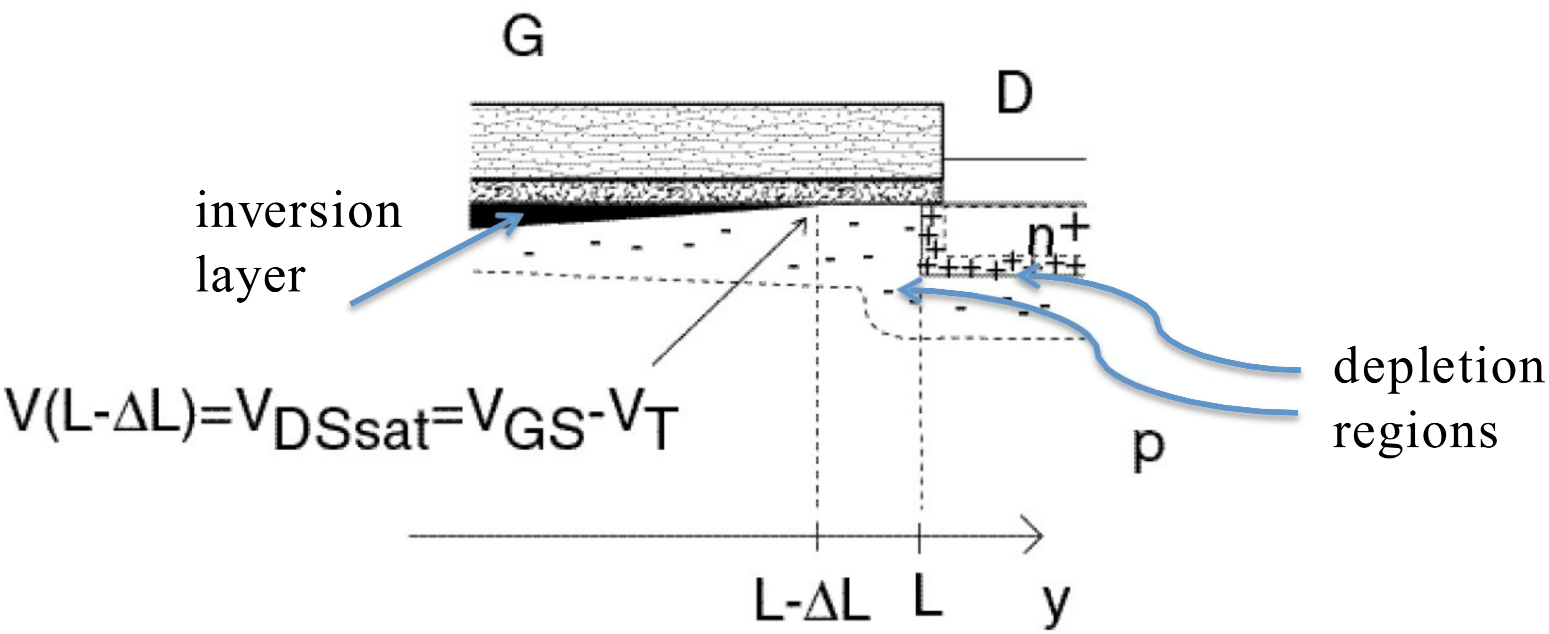
- Reverse-biased p-n junctions form a *depletion region*
  - Region between n (drain) and p (bulk) with no carriers
  - Width of depletion L_d region (between D and B) grows with reverse bias V_{db}
  - $L_{eff} = L - L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



Channel Length Modulation I/V (1/2)

- Increasing V_{ds} causes the depletion around the drain to widen.
- This pushes the pinch off point further away from the drain resulting in an effective shortening of the channel

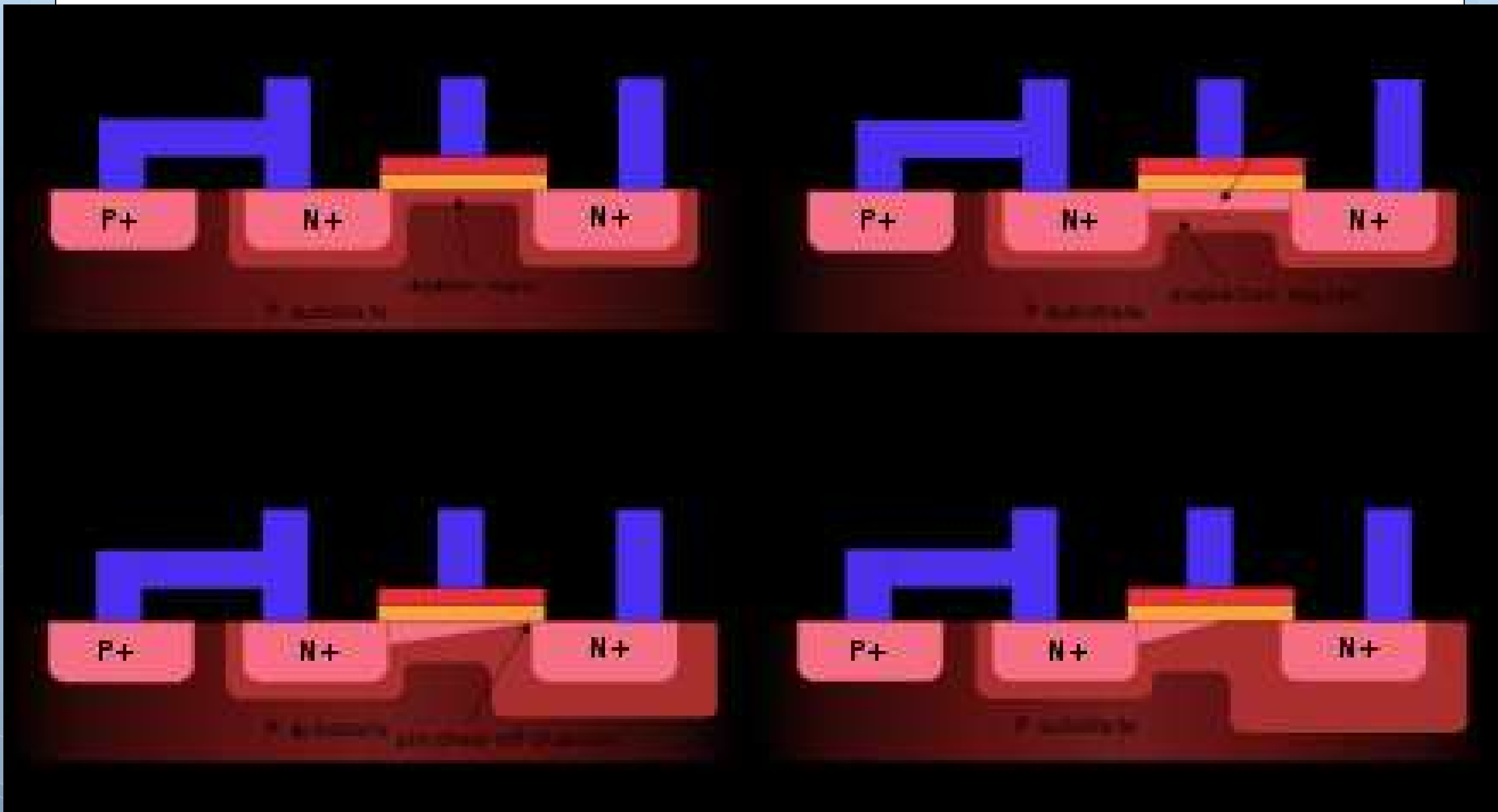
$\Delta L = L_d$



Channel Length Modulation IV(2/2)

$$I_{ds} \approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(1 + \lambda V_{ds}\right) (V_{gs} - V_t)^2$$

2


P+
N+
N+
P+
N+
N+
P+
N+
N+
P+
N+
N+

Lambda

- Lambda is inversely proportional to channel length

$$\lambda \propto \frac{1}{L}$$

- Lambda is a "fudge" factor (do not rely on a precise value of lambda)
- Improved but approximate model for the drain current in saturation:

$$I_{ds} \approx \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(1 + \lambda V_{ds}\right) \cdot \left(V_{gs} - V_t\right)^2 = \frac{\beta}{2} \cdot \left(1 + \lambda V_{ds}\right) \cdot \left(V_{gs} - V_t\right)^2$$

Electric Fields Effects

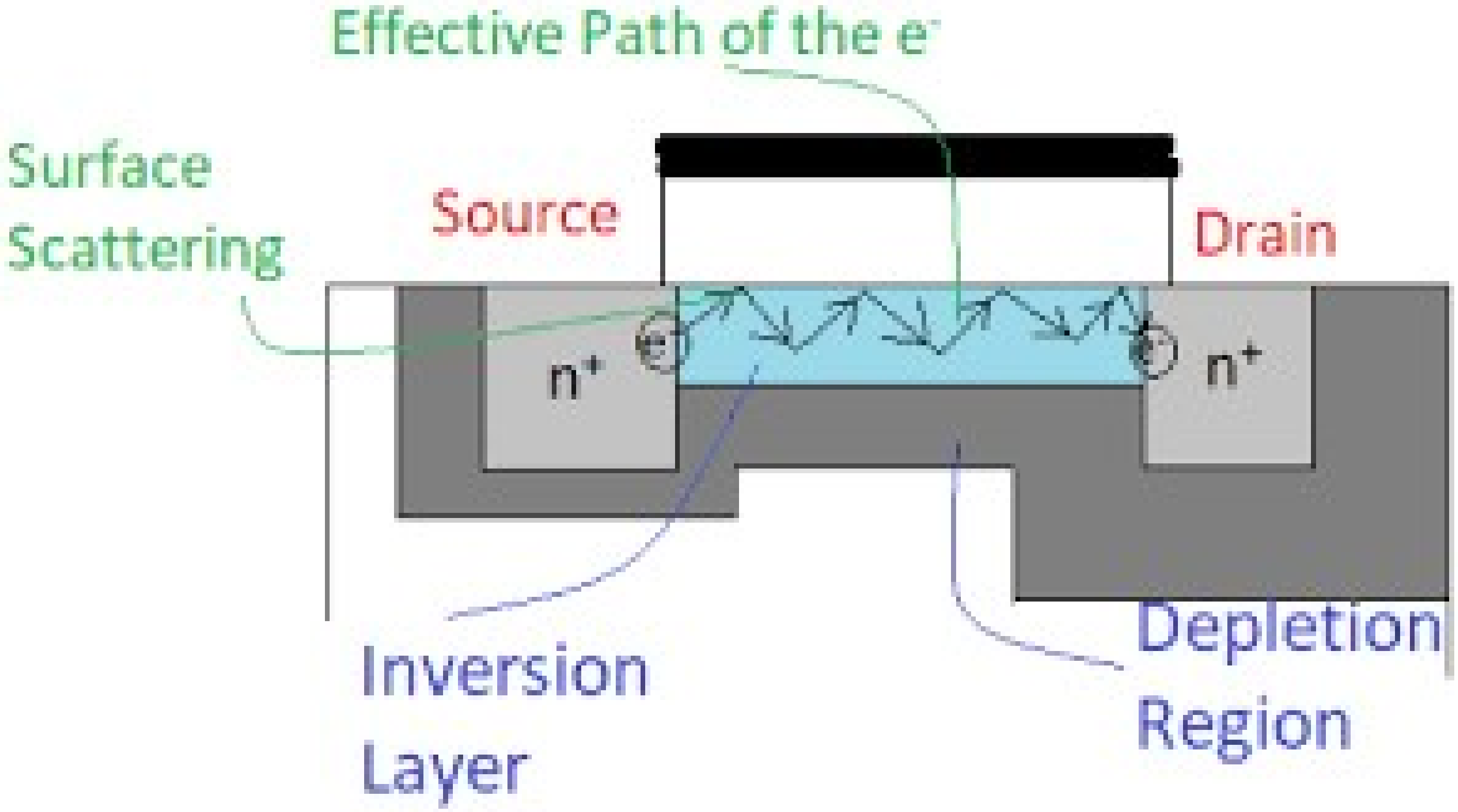
- **Mobility Degradation**
- **Velocity Saturation**

- Vertical electric field: $E_{vert} = V_{gs} / t_{ox}$
  - Attracts carriers into channel
  - Long channel: $Q_{channel} \propto E_{vert}$
- Lateral electric field: $E_{lat} = V_{ds} / L$
  - Accelerates carriers from drain to source
  - Long channel: $v = \mu E_{lat}$

Mobility Degradation

- High E_{vert} effectively reduces mobility
  - Collisions with oxide interface (at high V_{gs}, carriers are buffeted against the oxide interface "wall")

$$\mu_{\text{eff}-n} = \frac{540\,\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\left(\dfrac{V_{gs}+V_t}{0.54\,\frac{\text{V}}{\text{nm}}\,t_{\text{ox}}}\right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185\,\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\dfrac{\left|V_{gs}+1.5V_t\right|}{0.338\,\frac{\text{V}}{\text{nm}}\,t_{\text{ox}}}}$$

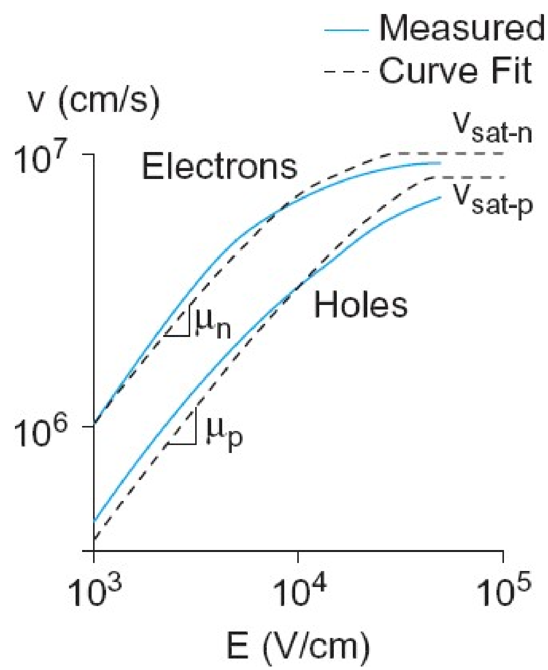


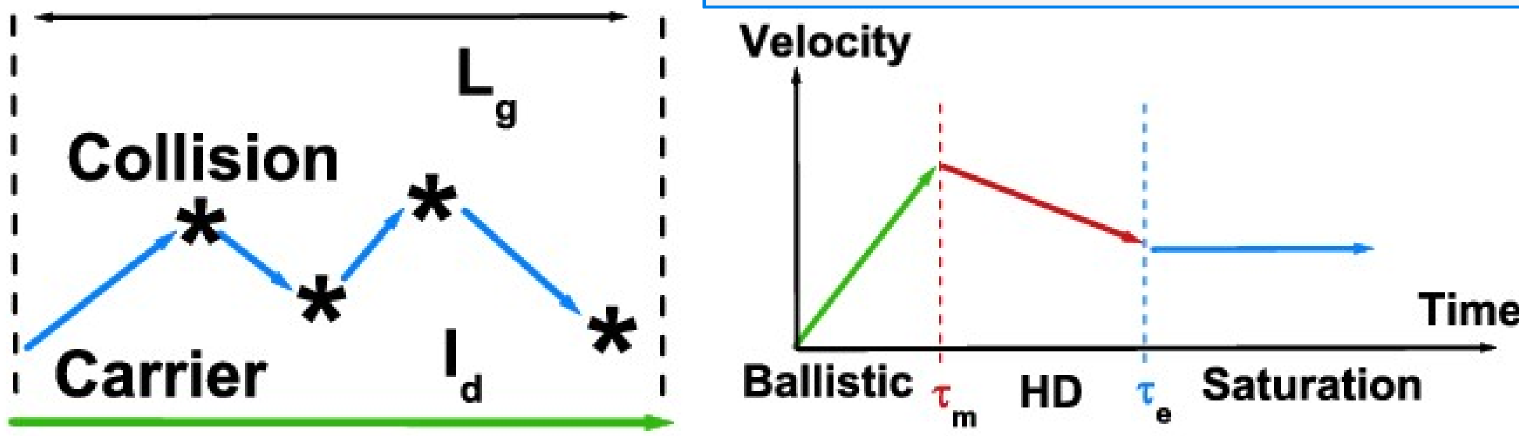
Effective Path of the e⁻
Surface Scattering
Source
Drain
n+
n+
Inversion Layer
Depletion Region

Velocity Saturation

- At high E_{lat}, carrier velocity rolls off
  - Carriers scatter off (collide) atoms in silicon lattice (at high E_{lat} the carriers effective mass increases)
  - Velocity reaches v_{sat}
    - Electrons: 10^7 cm/s
    - Holes: 8×10^6 cm/s
  - Better model

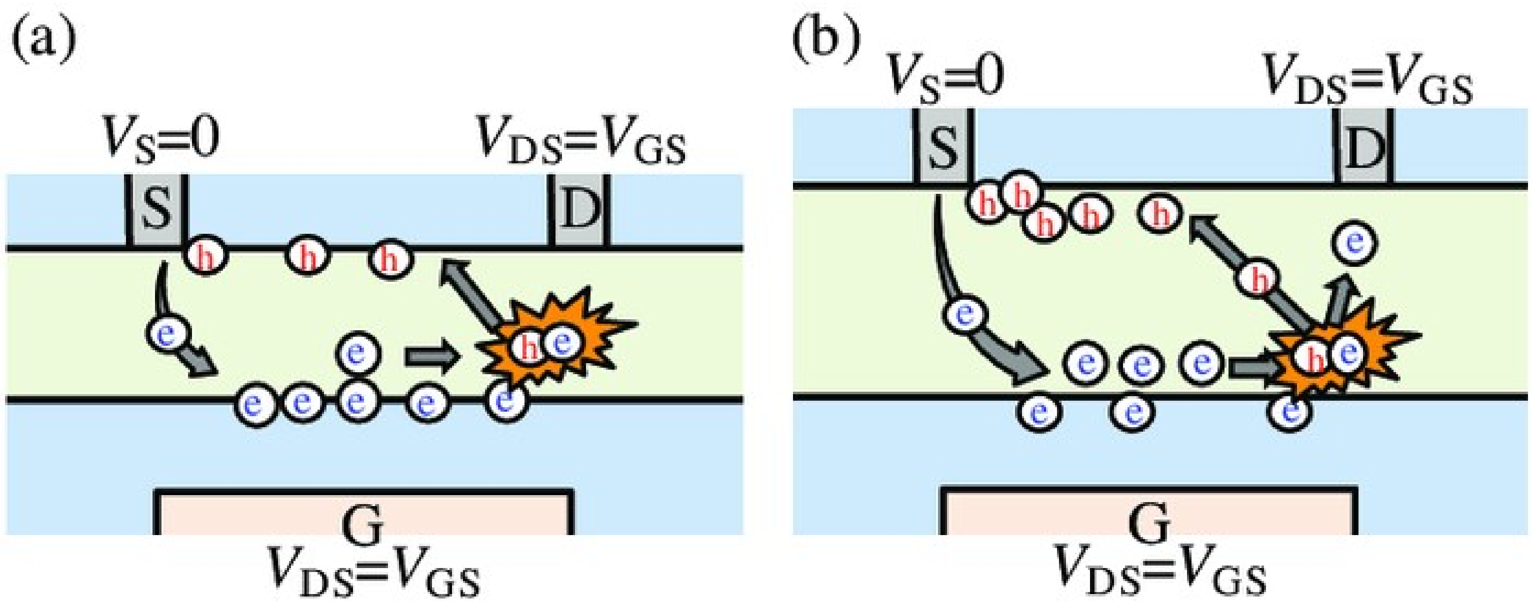
$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \qquad E_c = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}}$$





Lg
Collision
Carrier
ld
Velocity
Time
Ballistic
τm
HD
τe
Saturation

(a) (b)



(a)
VS=0
VDS=VGS
S
D
G
VDS=VGS
(b)
VS=0
VDS=VGS
S
D
G
VDS=VGS

Threshold Voltage Effects

- V_t is the value of V_{gs} for which the channel starts to invert
- Ideal models assume V_t is constant
- In reality it depends (weakly) on almost everything else:
  - Body voltage: *Body Effect*
  - Drain voltage: *Drain-Induced Barrier Lowering*
  - Channel length: *Short Channel Effect*

Body Effect

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{\Phi_s - V_{BS}} - \sqrt{\Phi_s}\right)$$

- The potential difference between source and body V_{SB} affects (increases) the threshold voltage
- Threshold voltage depends on:
  - V_{SB}
  - Process
  - Doping
  - Temperature

$$\gamma = \frac{\sqrt{2q\varepsilon_S N_{bulk}}}{\varepsilon_{ox}/t_{ox}} = Body\ \ Effect\ \ Coefficient \equiv GAMMA$$

$$\Phi_S = \frac{2KT}{q}\ln\frac{N_{bulk}}{n_i} = Surface\ \ Potential \equiv PHI$$

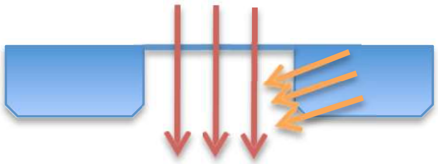
The higher the doping N_{bulk} the more voltage is required to produce an inversion layer: $N_{bulk}\uparrow \Rightarrow V_T\uparrow$

If C_{ox} is higher (= t_{ox} thinner) the less voltage is required to produce an inversion layer (Q=CV): $C_{ox}\uparrow \Rightarrow V_T\downarrow$

Body Effect

- V_{BS} affect the charge required to invert the channel
- For the same applied V_{GS}, the application of a negative V_{BS} *(we are only interested in a negative voltage to avoid forward biasing the bulk-to-source* pn junction) increases the width of the depletion region, thus the voltage required to invert the channel increases:

$$V_t = V_{t0} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$



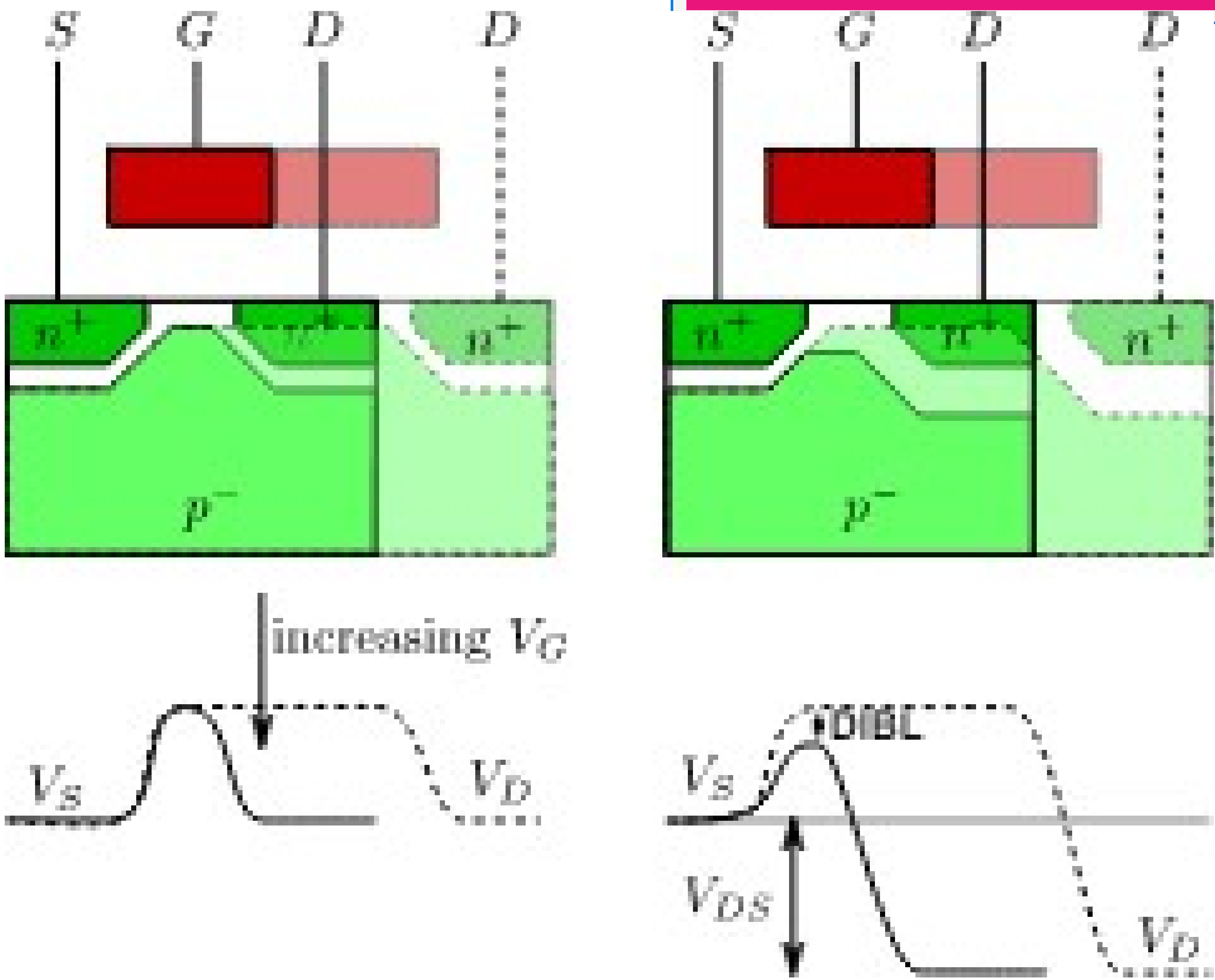
DIBL

- So far we assumed the amount of charge in the channel is controlled only by the vertical Iield
- For short transistors and especially small oxide thickness the amount of charge also depends on the later Iield. The drain is essentially like another “gate”.
- The drain cannot control the charge so well as the gate, but it also affect the amount of charge (and therefore the V_t)

$$V_t' = V_t - \eta V_{ds}$$

If η=0 then Vt= Vt
If not Vt=' decrease then Ids will increase

- High drain voltage causes current to increase


S
G
D
D
n^+
n^+
n^+
p^-
increasing V_G
V_S
V_D
S
G
D
D
n^+
n^+
n^+
p^-
DIBL
V_S
V_{DS}
V_D

Short Channel Effect

- In small transistors the source/drain depletion regions extend into a significant portion of the channel
  - impacts the amount of change required to invert the channel
  - V_t typically increases with L (some processes exhibit a reverse short channel effect)

Leakage

- What about current in cutoff ?

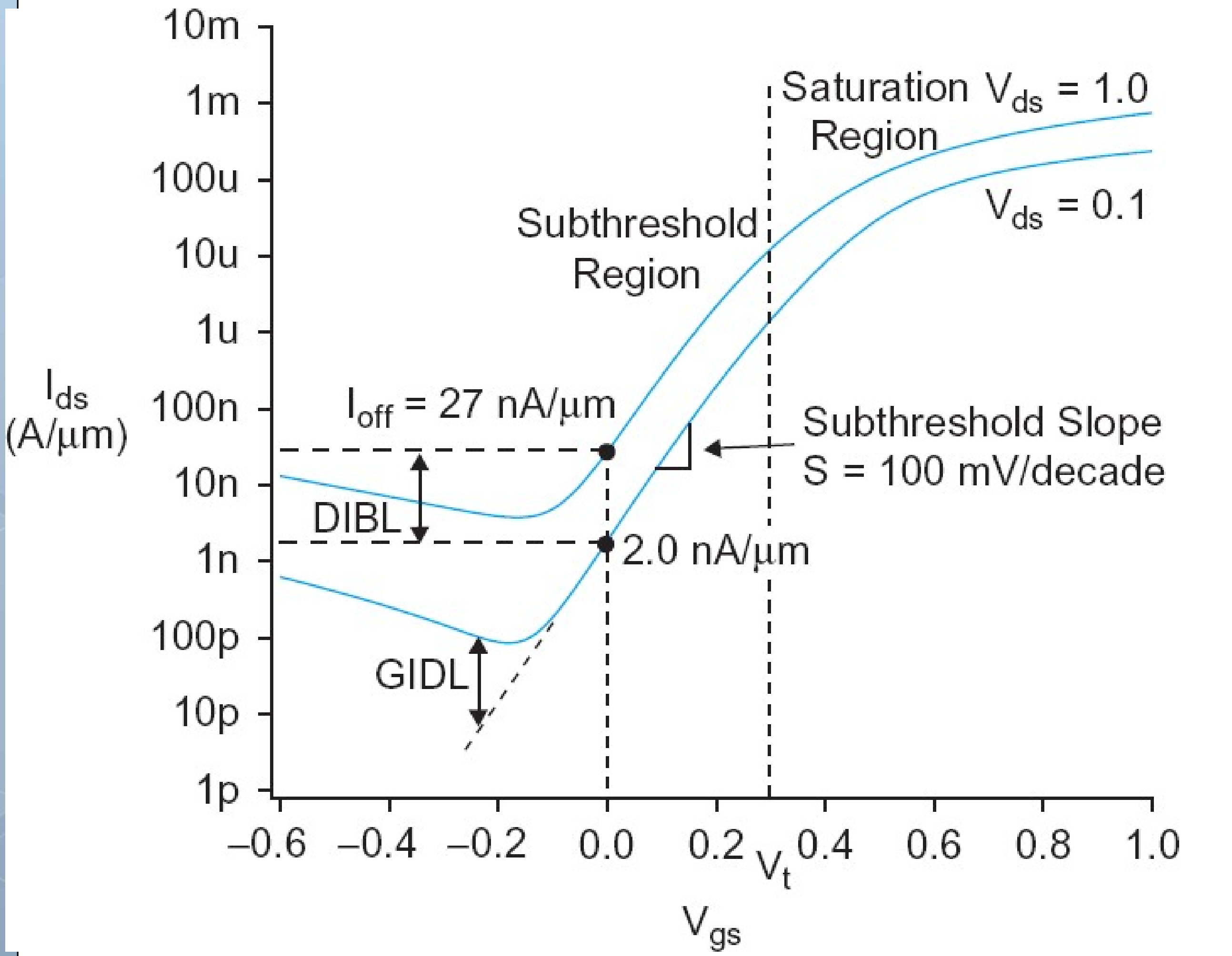
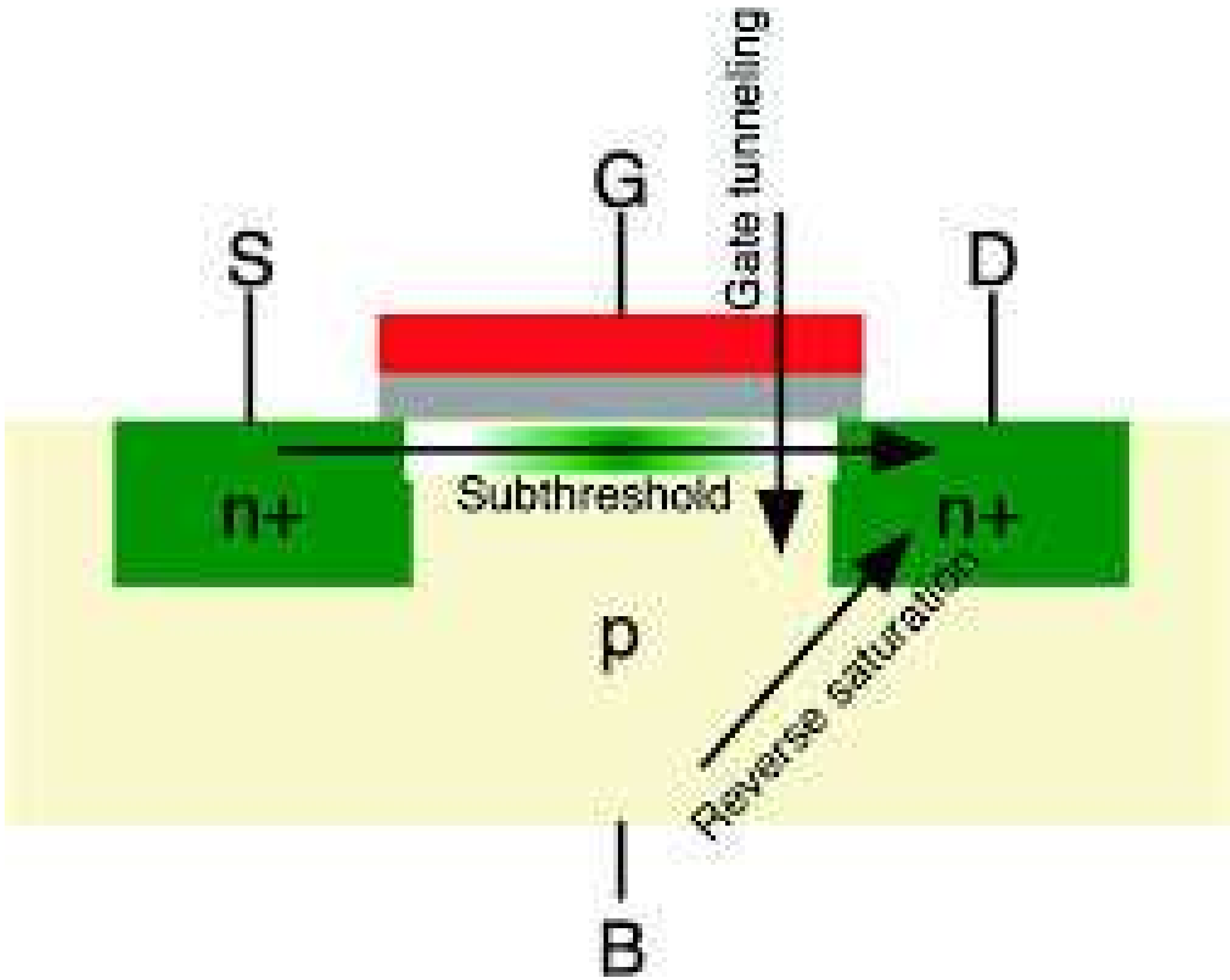


FIGURE 2.20 I-V characteristics of a 65 nm nMOS transistor at 70 °C on a log scale

Current doesn't go to 0 in cutoff !!!

Source of Leakage

- ***Subthreshold conduction***
  - Transistors can't abruptly turn ON or OFF
  - Dominant source in contemporary transistors
- ***Gate leakage***
  - Tunneling through ultrathin gate dielectric
- ***Junction leakage***
  - Reverse-biased PN junction diode current


G
S
D
Gate tunneling
n+
Subthreshold
n+
p
Reverse saturation
B

Subthreshold Conduction

- In real transistors, current doesn't abruptly cut off below threshold, but rather drop off exponentially with V_{GS}
- This leakage current when the transistor is nominally OFF depends on:
  - process (ε_{ox}, t_{ox}) → hidden in K_γ
  - doping levels (N_{bulk}) → hidden in K_γ
  - device geometry (W, L) → hidden in I_{ds0}
  - temperature (T) → hidden in v_T=KT/q
  - Subthreshold voltage (V_t)

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_\gamma V_{sb}}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right)$$

n is process dependent, typically 1.3–1.7

Gate Leakage

$$I_{gate} = WA\left(\frac{V_{DD}}{t_{ox}}\right)^2 e^{-B\frac{t_{ox}}{V_{DD}}}$$

A and B are tech constants

- There is a finite probability that carriers will tunnel through the thin gate oxide. This result in gate leakage current flowing into the gate. I_{gate} is greater for electrons (nMOS gates leak more)
- The probability drops off exponentially with t_{ox}
- For oxides thinner than 15-20Å, tunneling becomes a critically important factor (at 65nm $t_{ox} \approx 10.5$ Å)

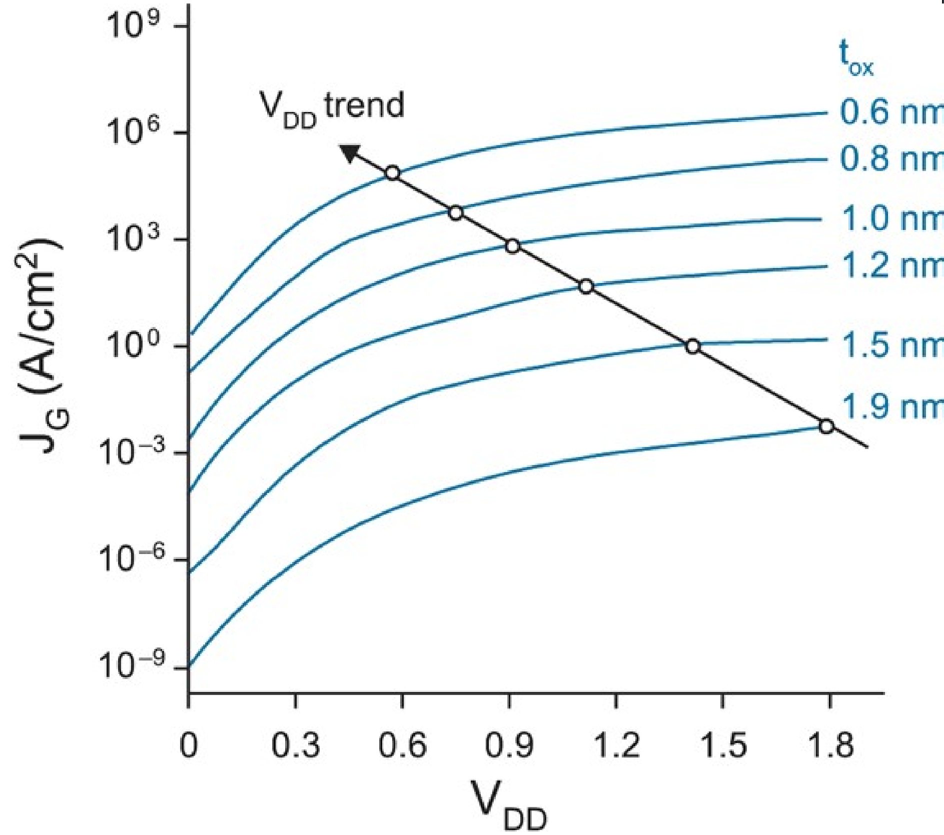


FIG 2.20 Gate leakage current from [Song01]

Junction Leakage

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- The pn junctions between diffusion and the substrate or well for diodes.
- The well-to-substrate is another diode
- Substrate and well are tied to GND and VDD to ensure these diodes remain reverse biased
- But, reverse biased diodes still conduct a small amount of current that depends on: (I_S is typically < 1fA/μm^2)
  - Doping levels
  - Area and perimeter of the diffusion region
  - The diode voltage

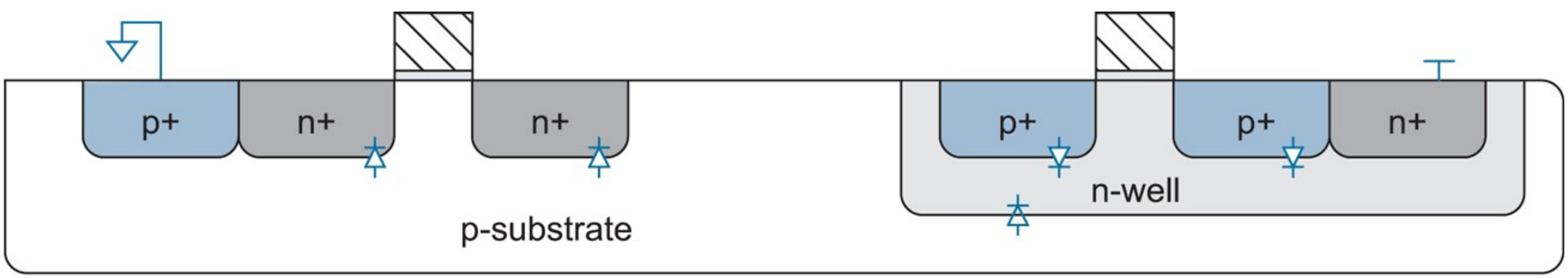
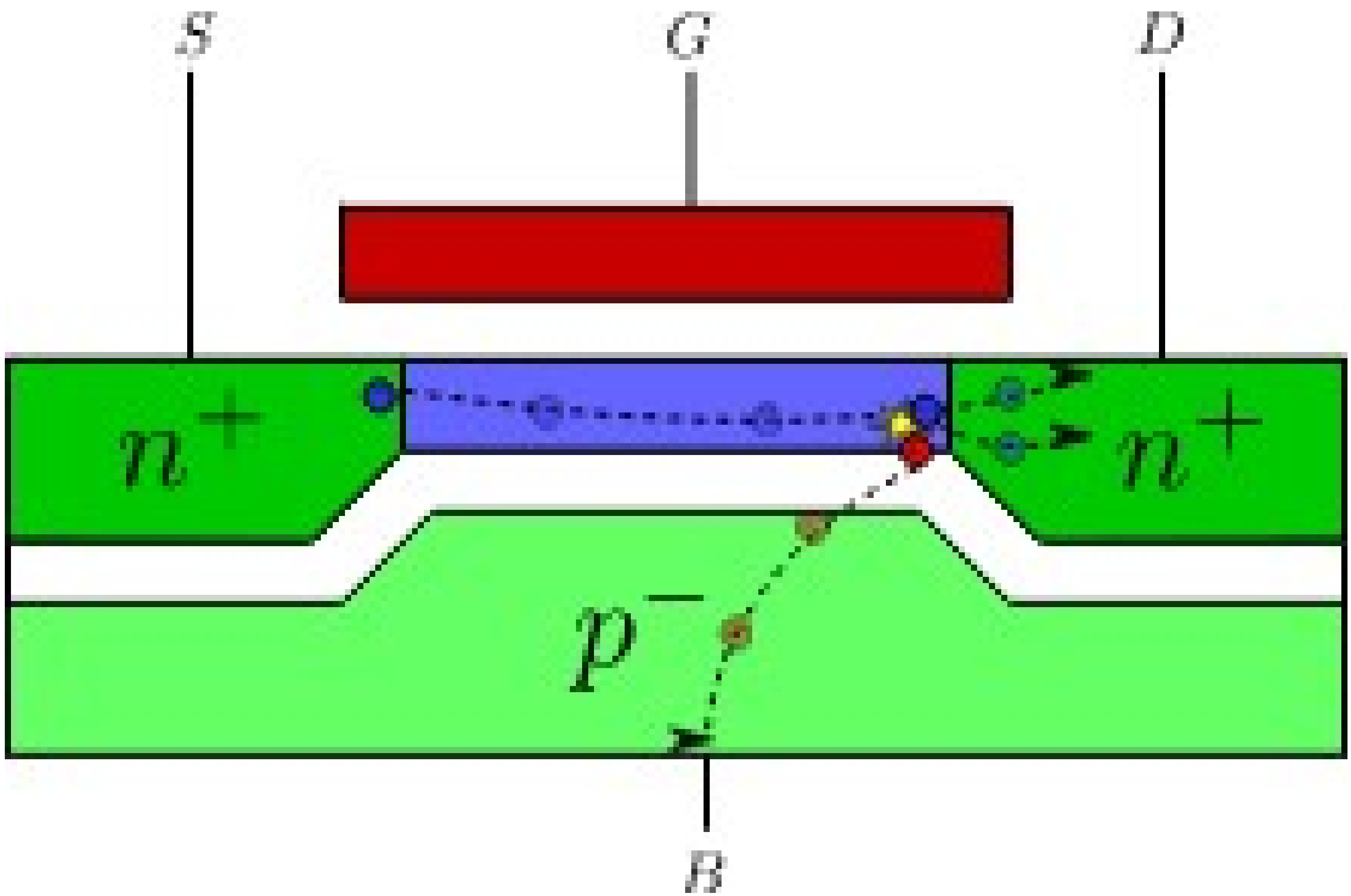


FIG 2.19 Reverse-biased diodes in CMOS circuits



S
G
D
n+
n+
p−
B

Temperature dependence

- Transistor characteristics are influenced by temperature
  - μ decreases with T
  - V_t decreases linearly with T
  - $I_{leakage}$ increases with T
- ON current decreases with T
- OFF current increases with T
- Thus, circuit performances are worst at high temperature

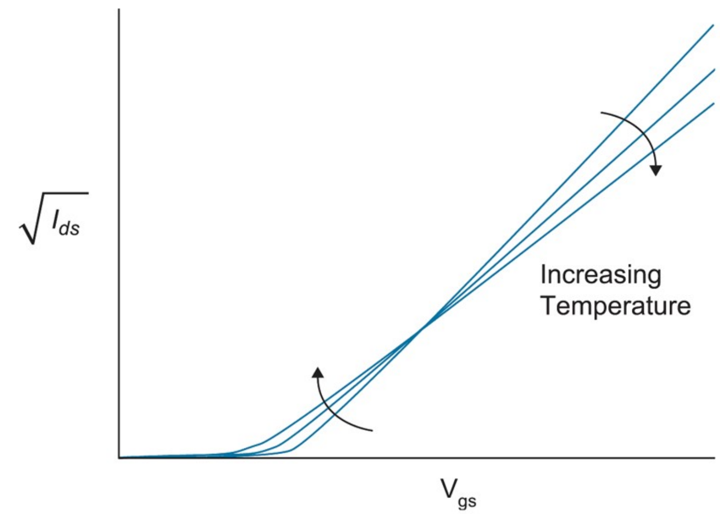


FIG 2.21 I–V characteristics of nMOS transistor in saturation at various temperatures

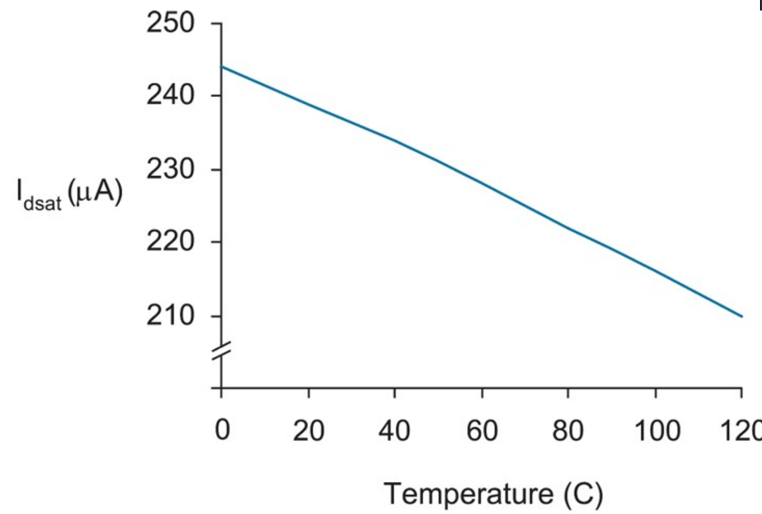


FIG 2.22 I_{dsat} vs. temperature

Geometry Dependence

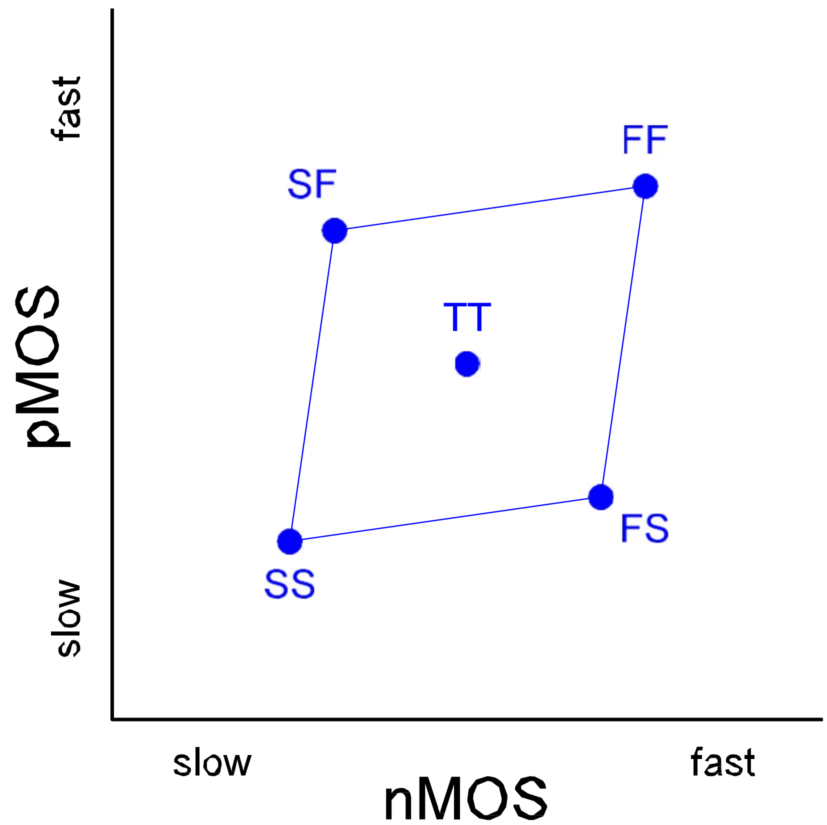
- Layout designers draw transistors with W_{drawn} L_{drawn}
- Actual dimensions may differ from some factor X_W and X_L
- The source and drain tend to diffuse laterally under the gate by L_D, producing a shorter effective channel
- Similarly, diffusion of the bulk by W_D decreases the effective channel width
- In process below 0.25 µm the effective length of the transistor also depends significantly on the orientation of the transistor

$$L_{eff} = L_{drawn} + X_L - 2L_D$$

$$W_{eff} = W_{drawn} + X_W - 2W_D$$

Process Variation

- Transistors have uncertainty in process parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
- Variation is around typical (T) values
- Fast (F)
  - L_{eff}: short
  - V_t: low
  - t_{ox}: thin
- Slow (S): opposite
- Not all parameters are independent for nMOS and pMOS



Environmental Variation

- V_{DD} and *Temperature* also vary in *time* and *space*
- *Fast:*
  - V_{DD}: high
  - T: low

Corner	Voltage	Temperature
F	1.98	0 C
T	1.8	70 C
S	1.62	125 C

Process Corners

- Process corners describe worst case variations
  - If a design works in all corners, it will ***probably*** work for any variation.
- Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

Important Corners

- Critical Simulation Corners include

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time	S	S	S	S
Power	F	F	F	F
Subthreshold leakage	F	F	F	S

Impact of non-ideal V effects

- Threshold is a signiIicant fraction of the supply voltage
- Leakage is increased causing gates to
  - consume power when idle
  - limits the amount of time that data is retained
- Leakage increases with temperature
- Velocity saturation and mobility degradation result in less current than expected at high voltage
  - No point in trying to use high VDD to achieve fast transistors
  - Transistors in series partition the voltage across each transistor thus experience less velocity saturation
    - Tend to be a little faster than a single transistor
    - Two nMOS in series deliver more than half the current of a single nMOS transistor of the same width
- Matching: same dimension and orientation

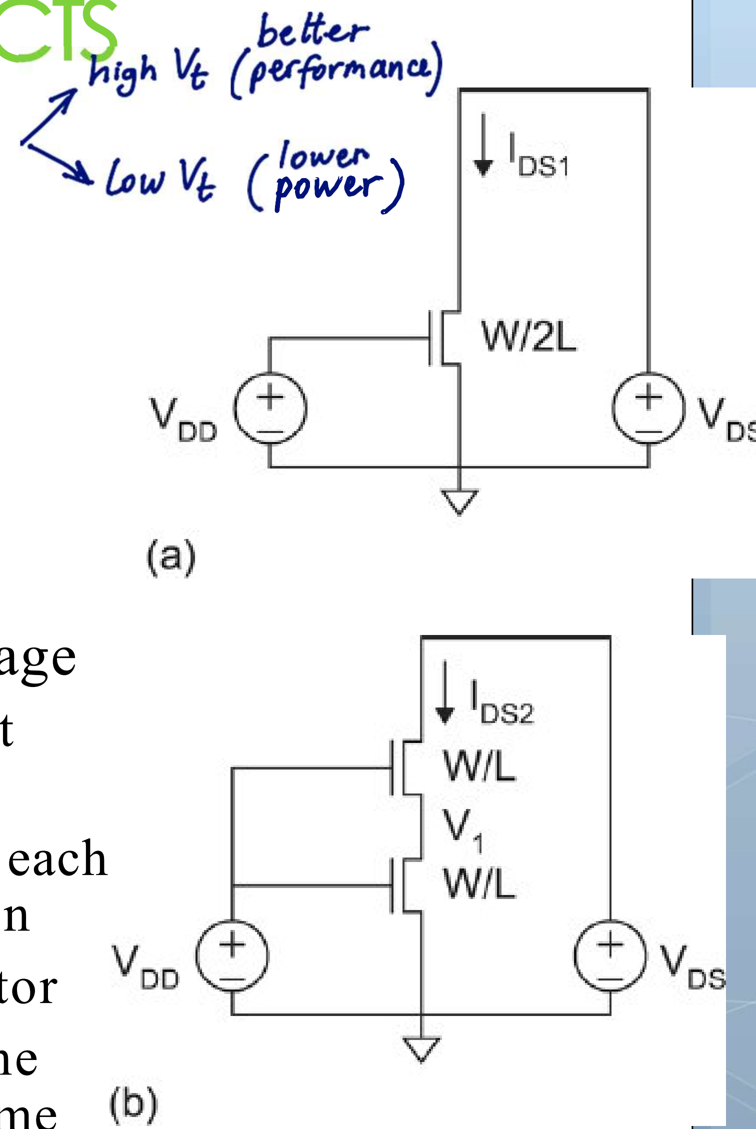


FIG 2.37 Current in series transistors

So What?

- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Logical effort
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation

Dynamic Behavior or CV Charac

- Gate capacitance –

  gate –electrode 1

  Oxide- dielectric

  Channel - electrode 2

Required for MOSFET operation

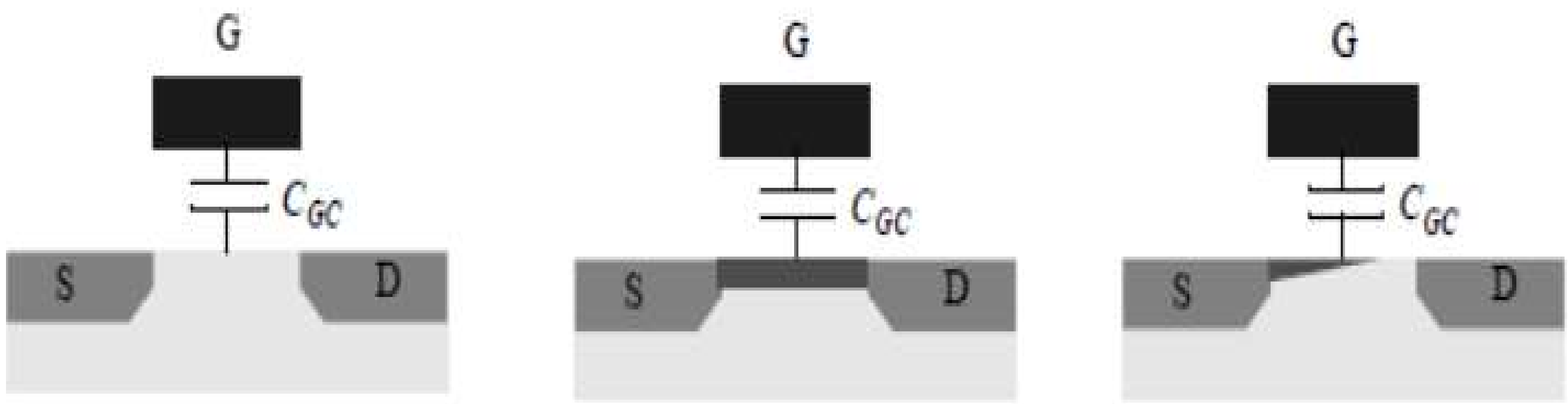
- Parasitic Capacitance

  pn junction

  Diffusion (s or D) –electrode 1

  Depletion region- dielectric

  Body or substrate -- electrode 2

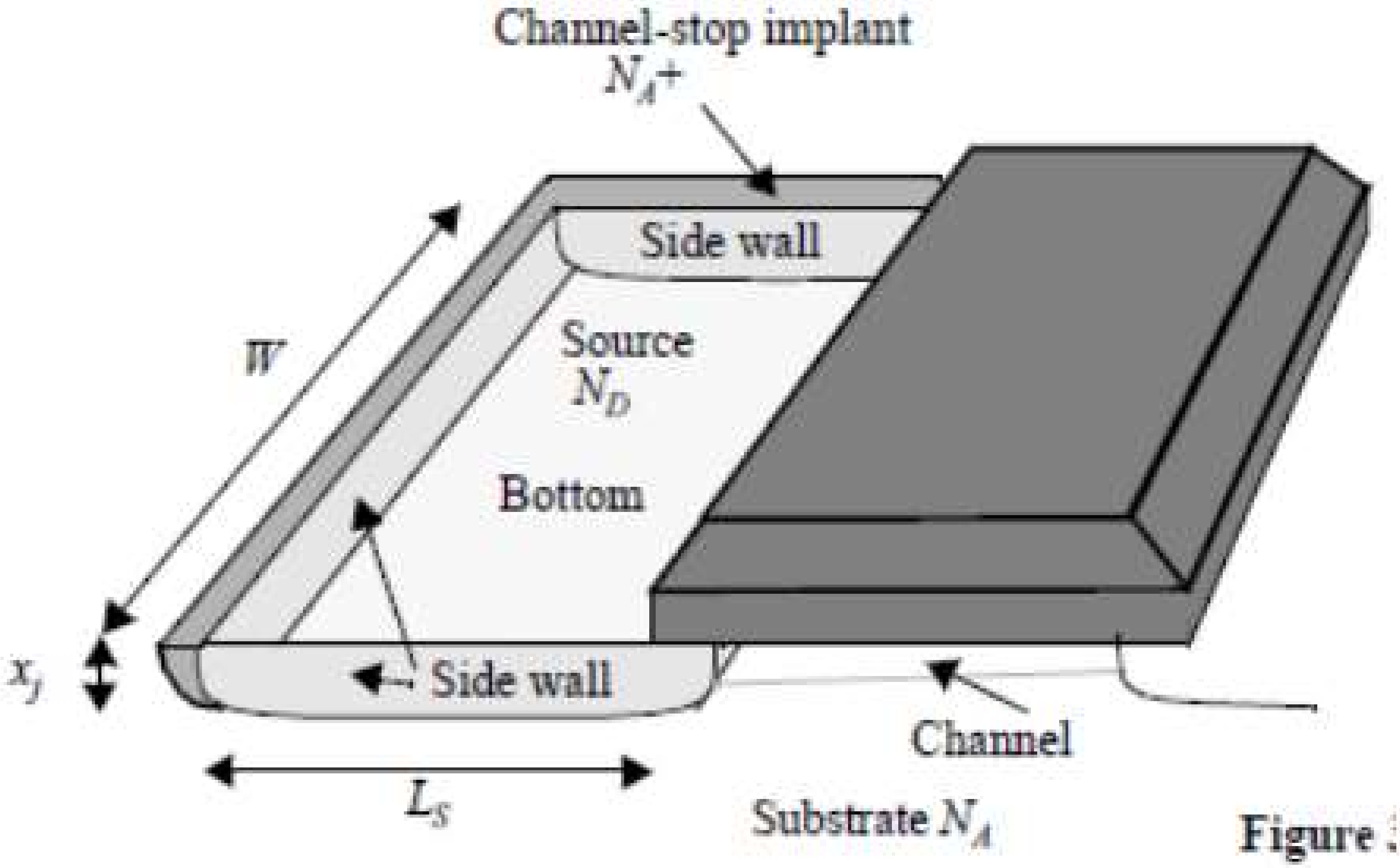


(a) cut-off (b) resistive (c) saturation

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Cutoff	$C_{ox}WL$	0	0	$C_{ox}WL$	$C_{ox}WL+2C_oW$
Resistive	0	$C_{ox}WL / 2$	$C_{ox}WL / 2$	$C_{ox}WL$	$C_{ox}WL+2C_oW$
Saturation	0	$(2/3)C_{ox}WL$	0	$(2/3)C_{ox}WL$	$(2/3)C_{ox}WL+2C_oW$

Junction Capacitances

- reverse-biased source-body
- drain body pn-junctions.



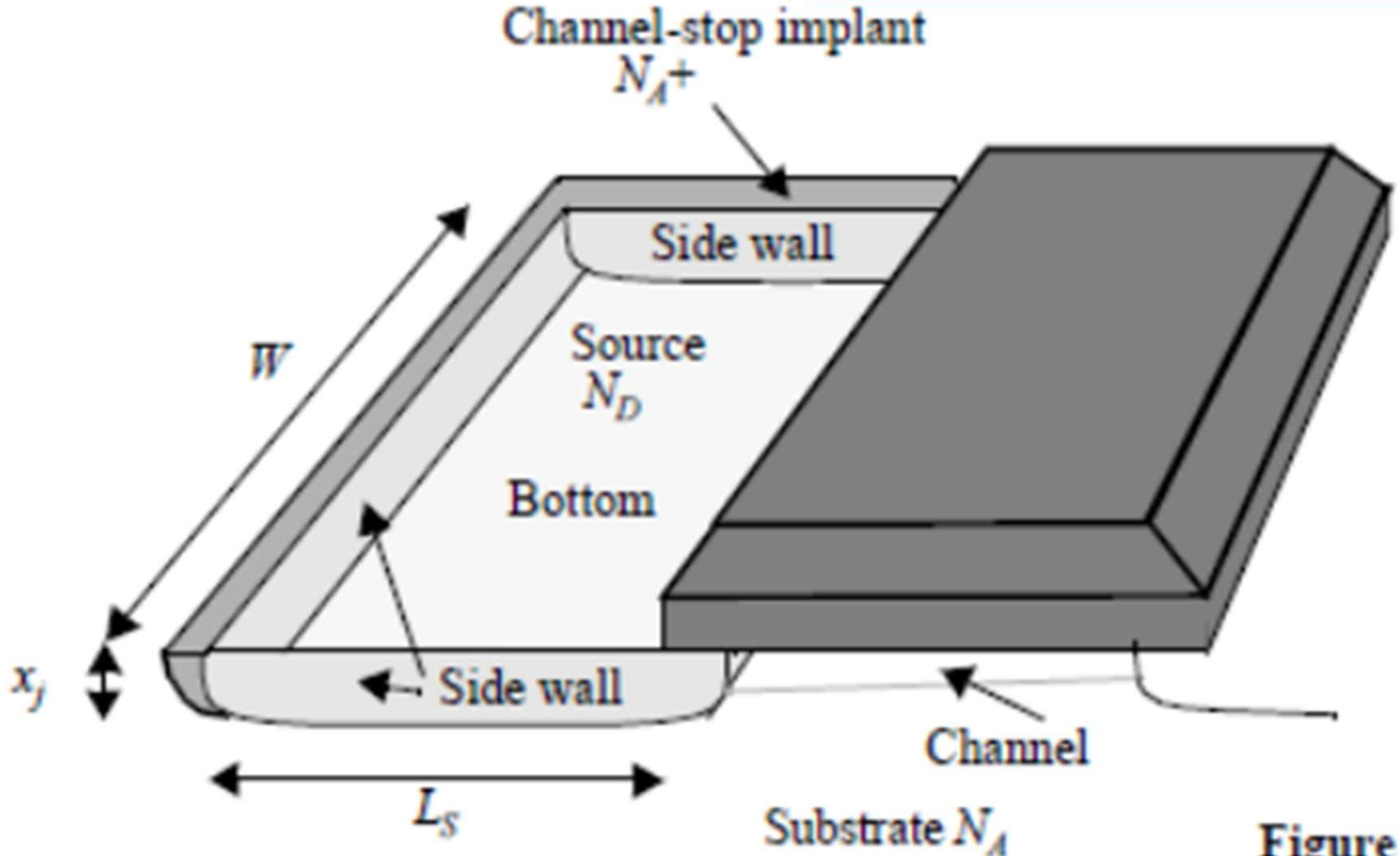
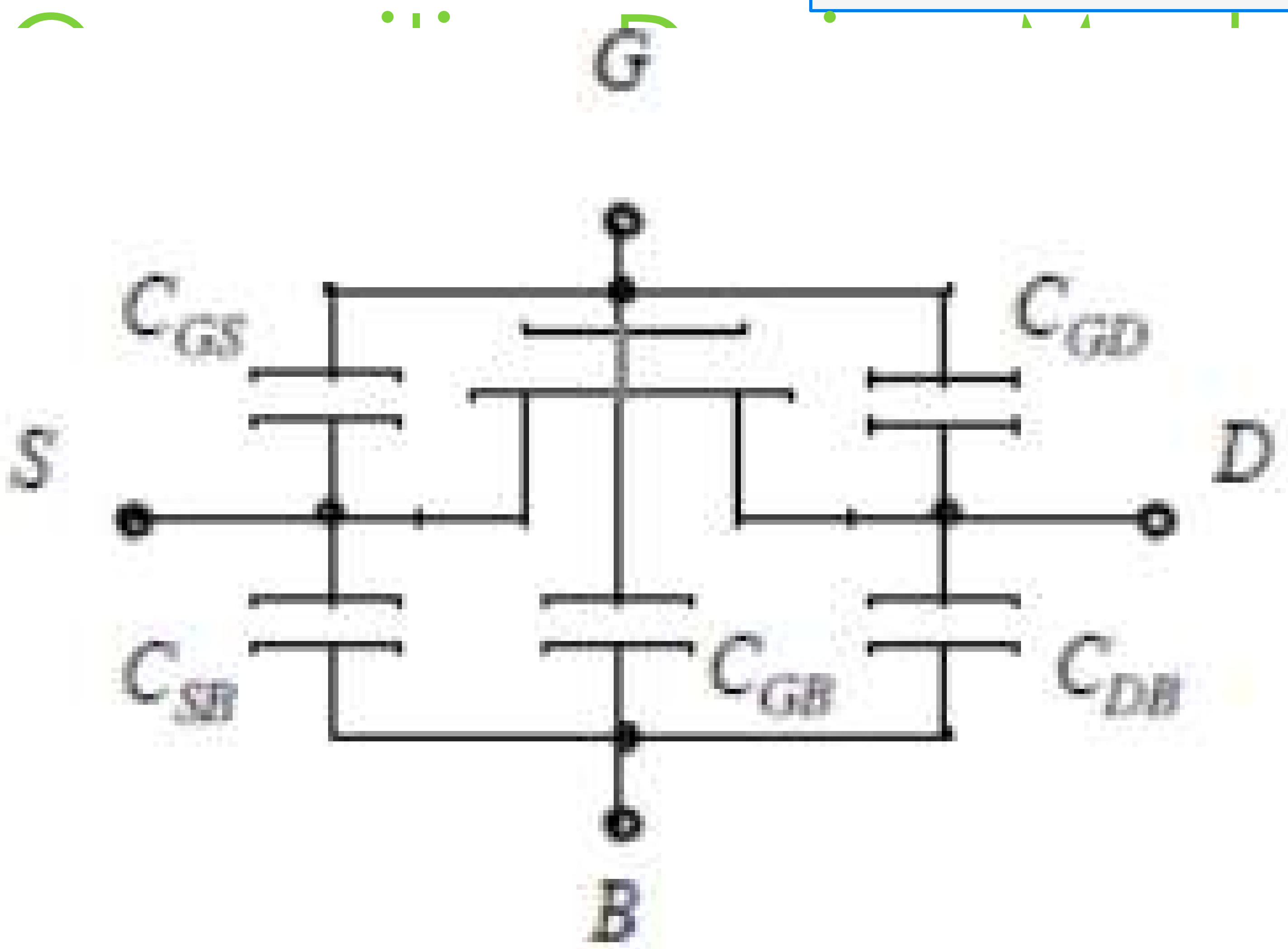


Figure :

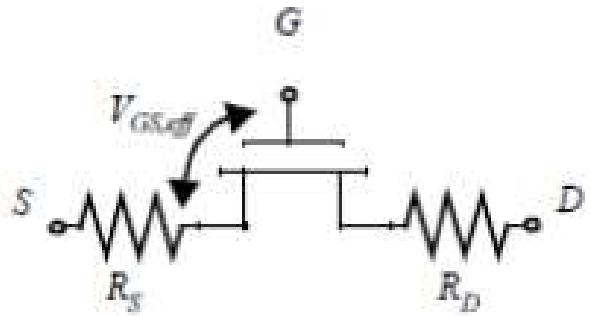
$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$



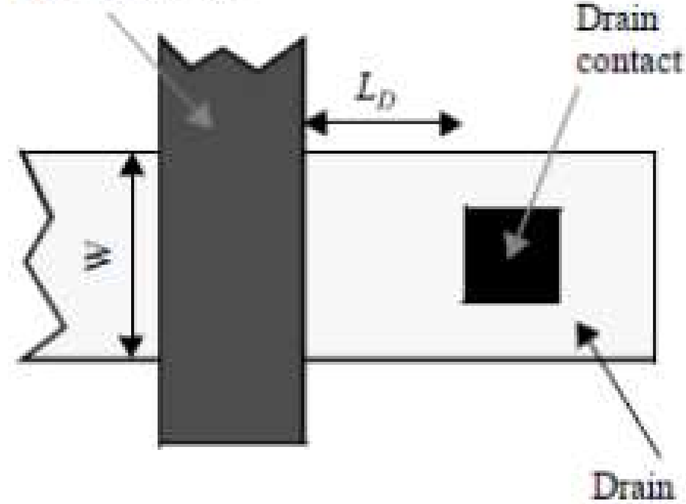
$$C_{GS} = C_{GCS} + C_{GSO};\ C_{GD} = C_{GCD} + C_{GDO};\ C_{GB} = C_{GCB}$$

$$C_{SB} = C_{Sdiff};\ C_{DB} = C_{Ddiff}$$

Source-Drain Resistance



(a) Modeling the series resistance

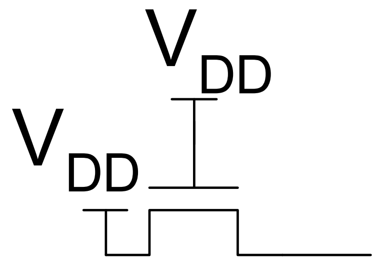


(b) Parameters of the series resistance

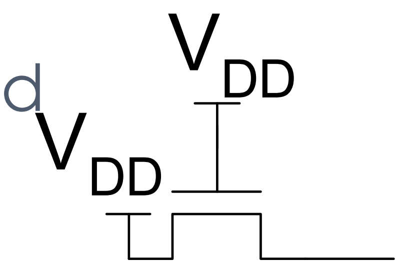
$$R_{S,D} = \frac{L_{S,D}}{W} R_{\square} + R_C$$

Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing V_{DD}

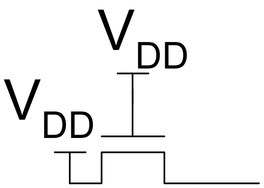


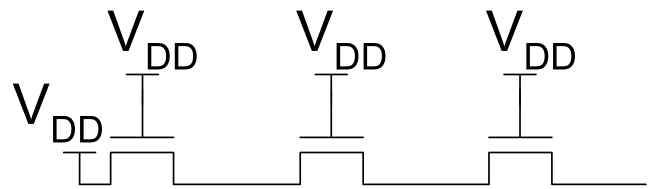
Pass Transistors

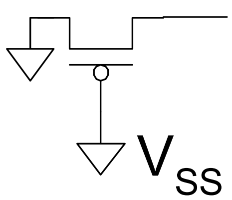


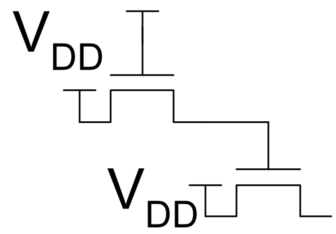
- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing V_{DD}
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded "1"
  - Approach degraded value slowly (low I_{ds})
- pMOS pass transistors pull no lower than V_{tp}

Pass Transistor Ckts

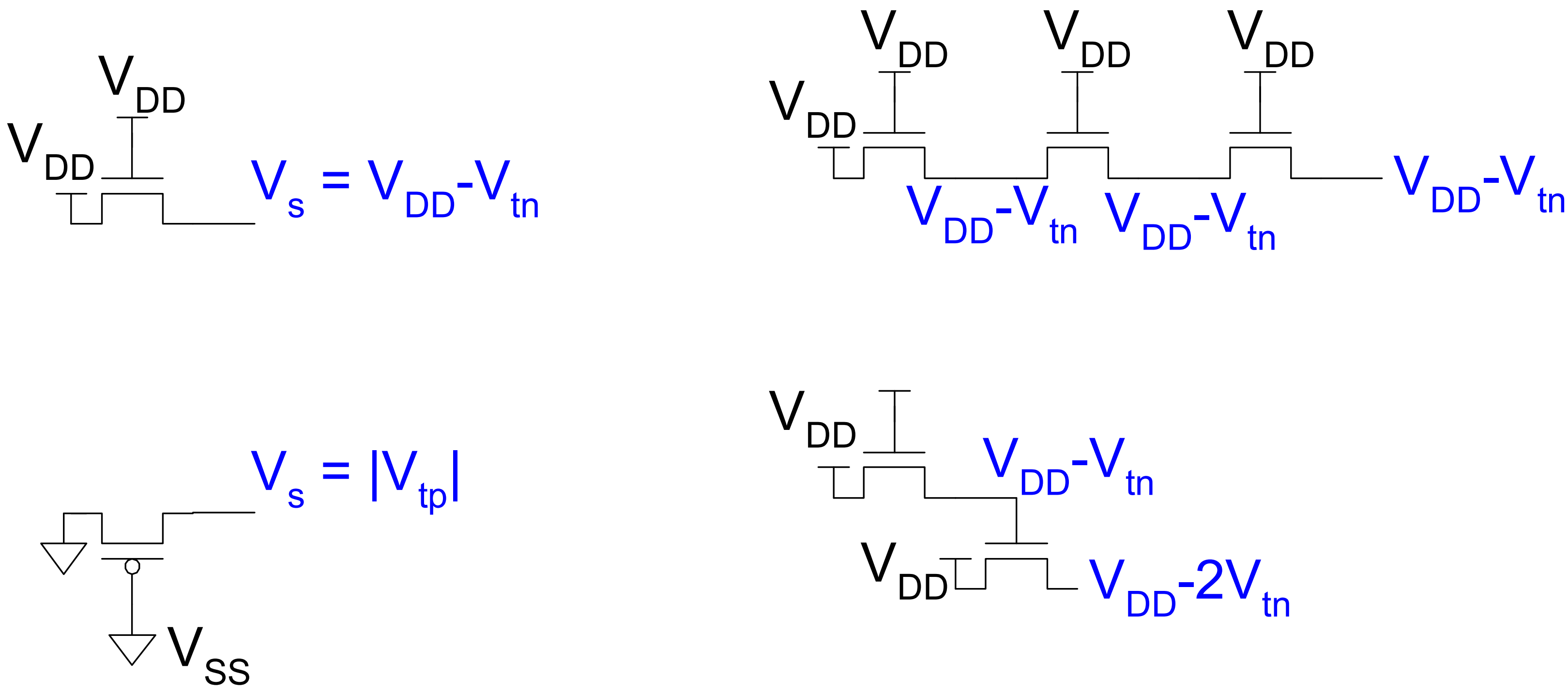


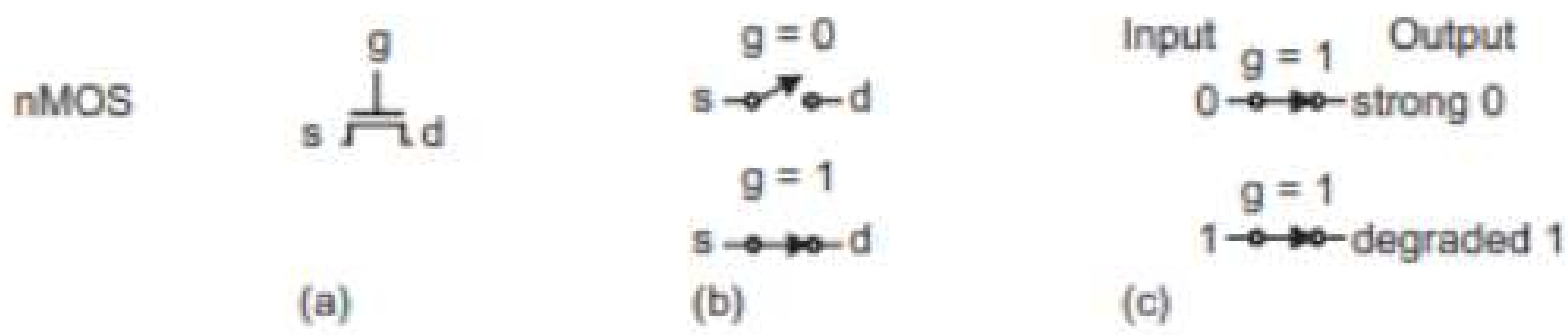




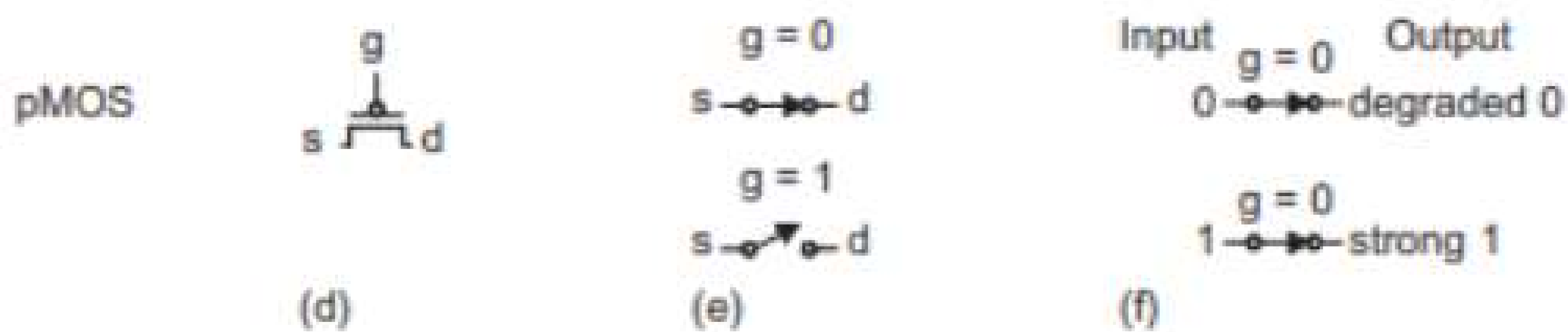


Pass Transistor Ckts

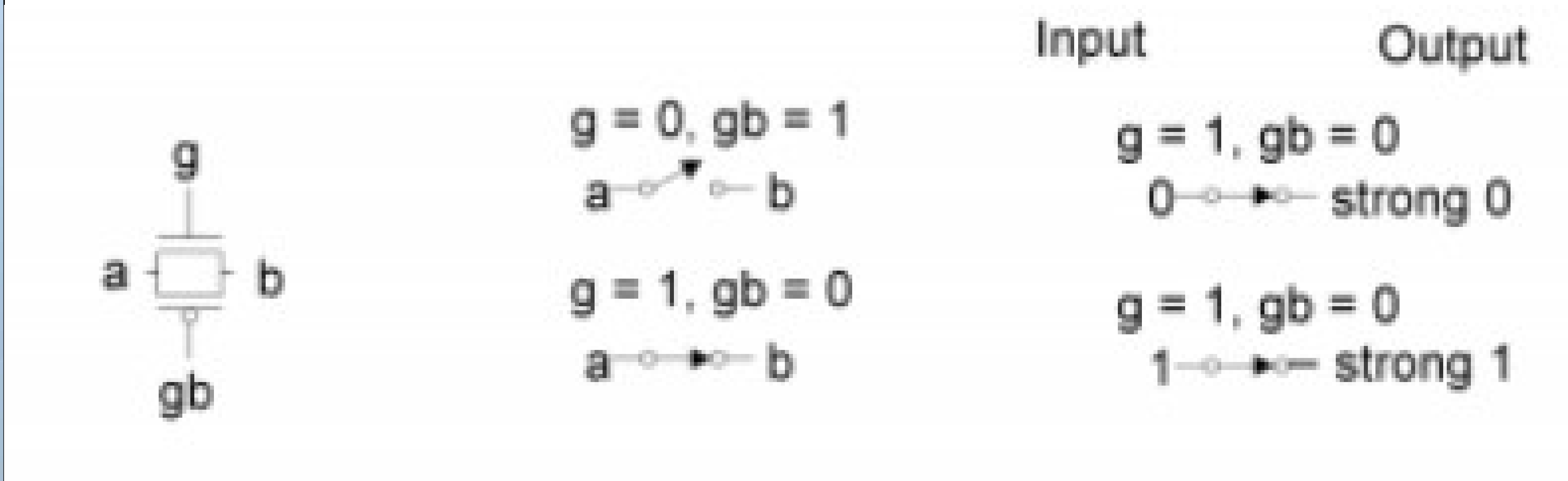




nMOS – Gate=1 ---ON , o/p = i/p
pMOS – Gate = 0 ---ON , o/p = i/p

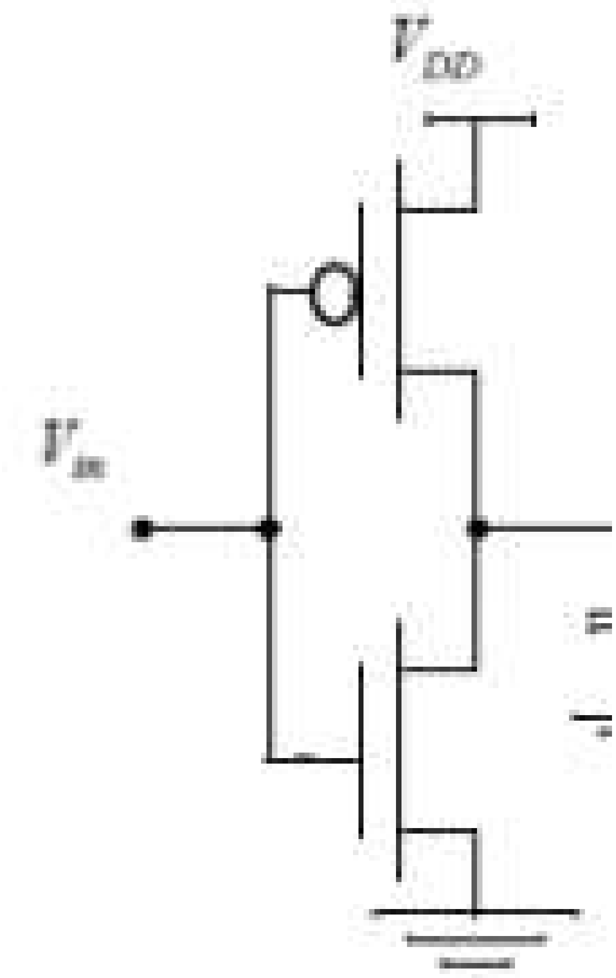


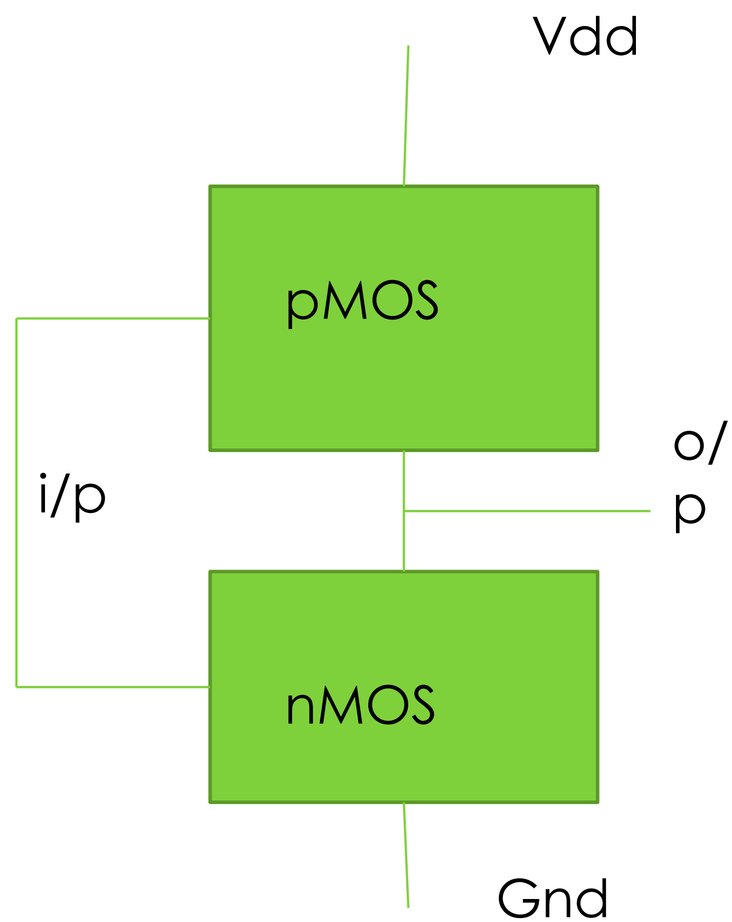
Transmission Gate



- Passes Strong 0 and strong 1
- nMOS – Gate=1 ---ON , o/p = i/p
- pMOS – Gate = 0 ---ON , o/p = i/p

CMOS logic





- nMOS –

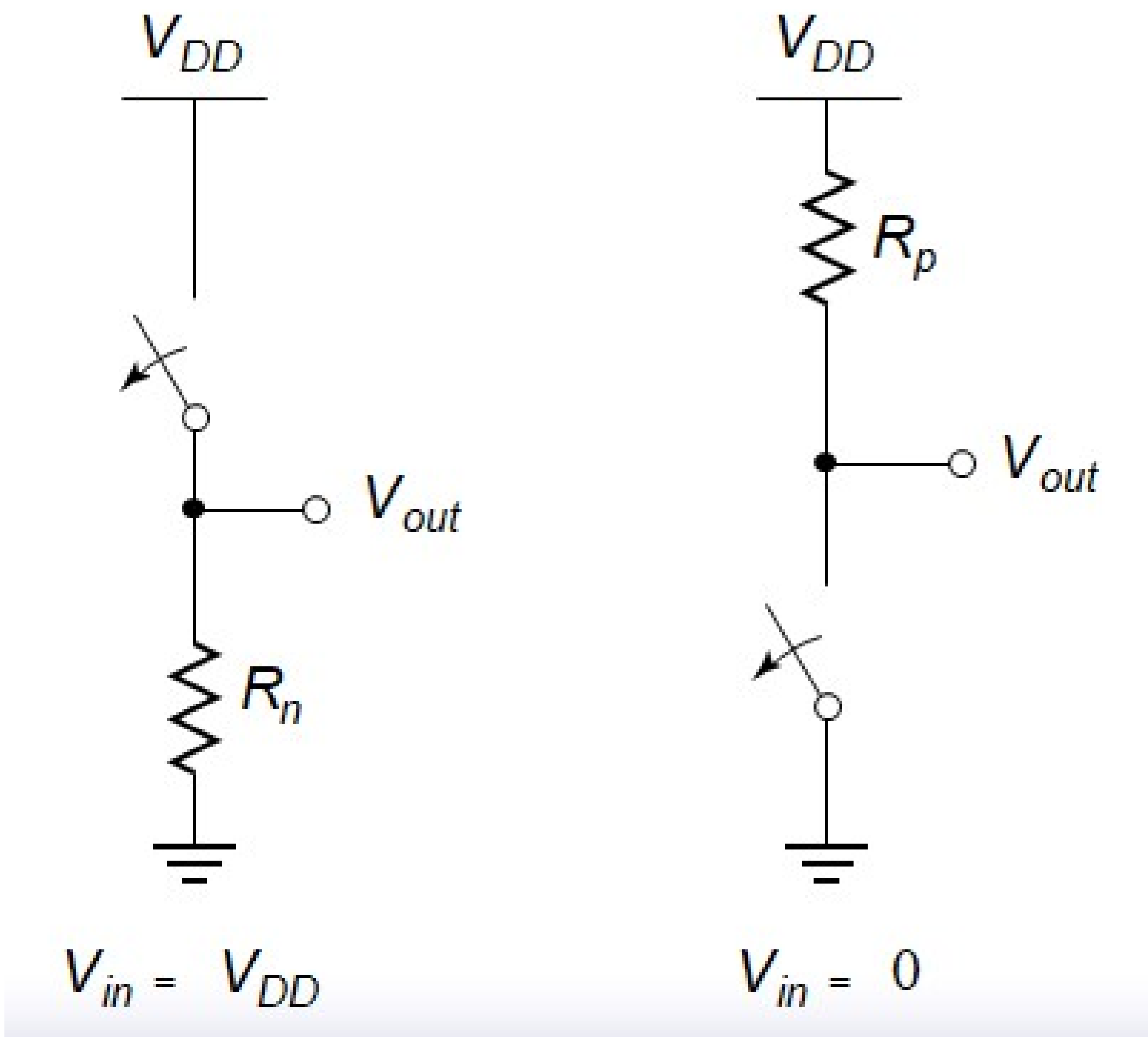
  Gate=1 ---ON , SC

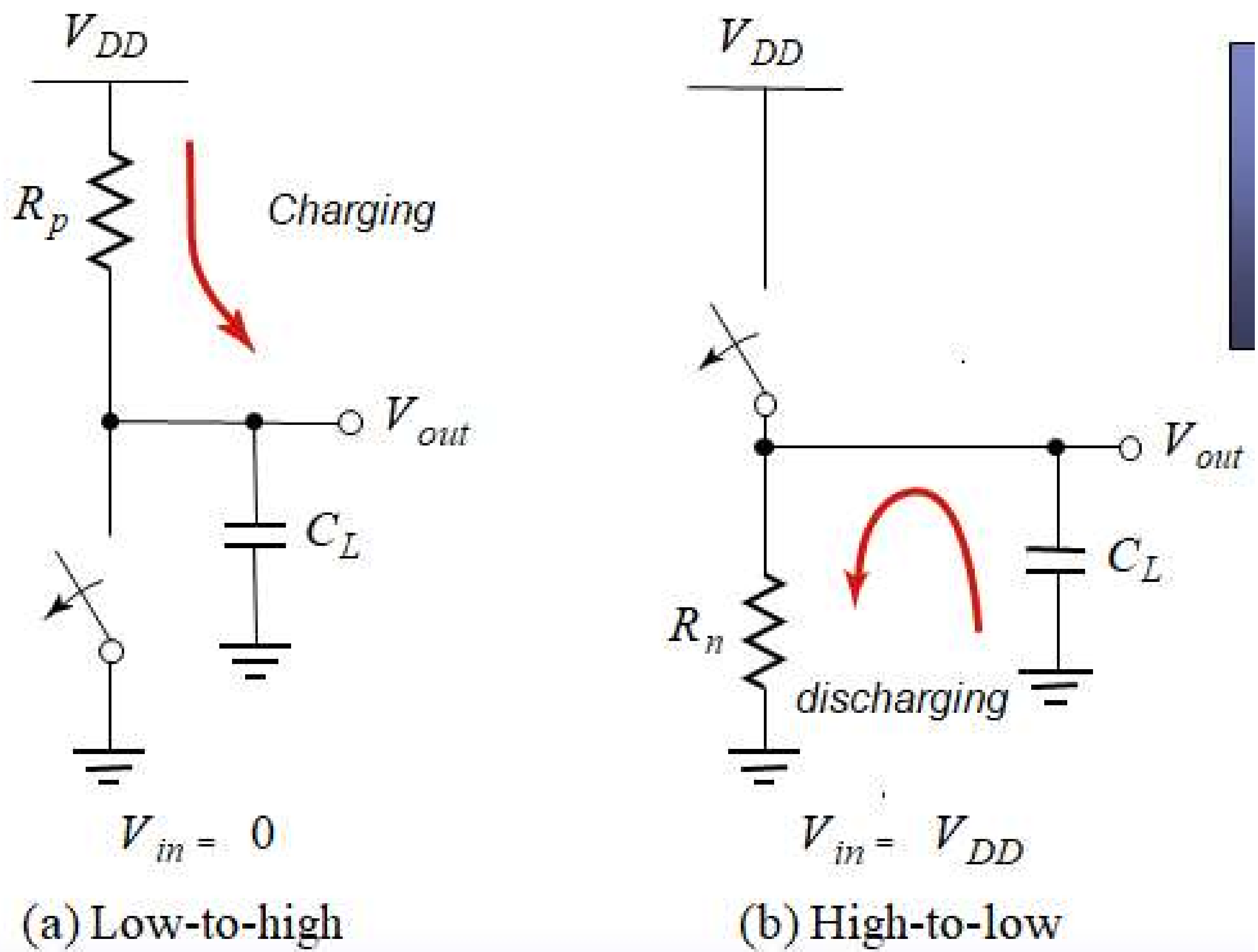
  Gate=0 ---OFF , OC

- pMOS –

  Gate = 0 ---ON , SC

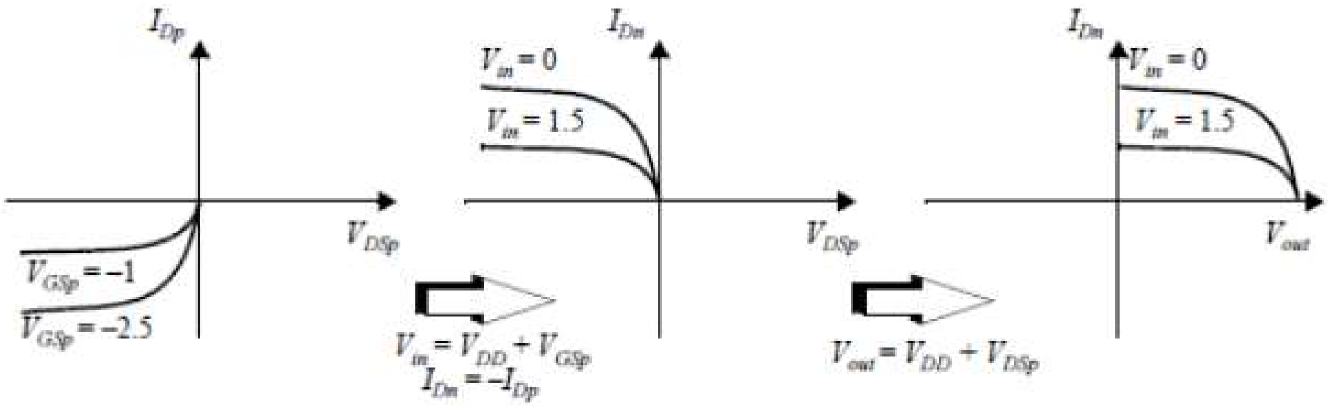
  Gate = 1 ---OFF , OC

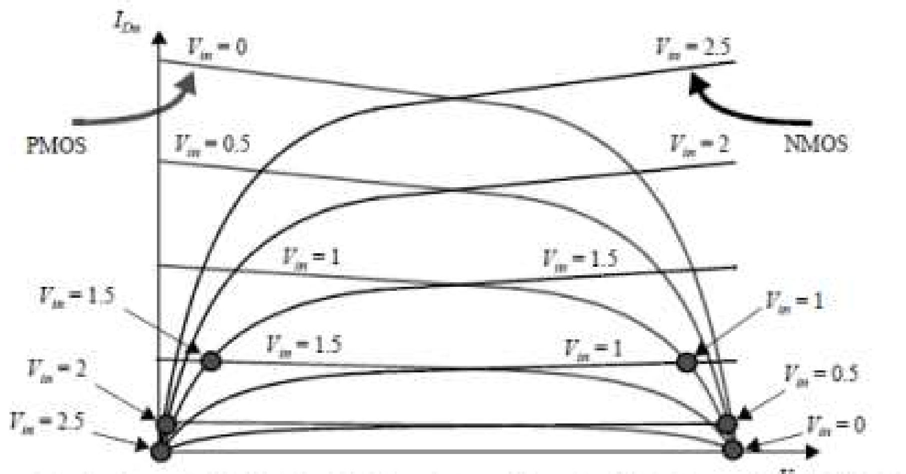


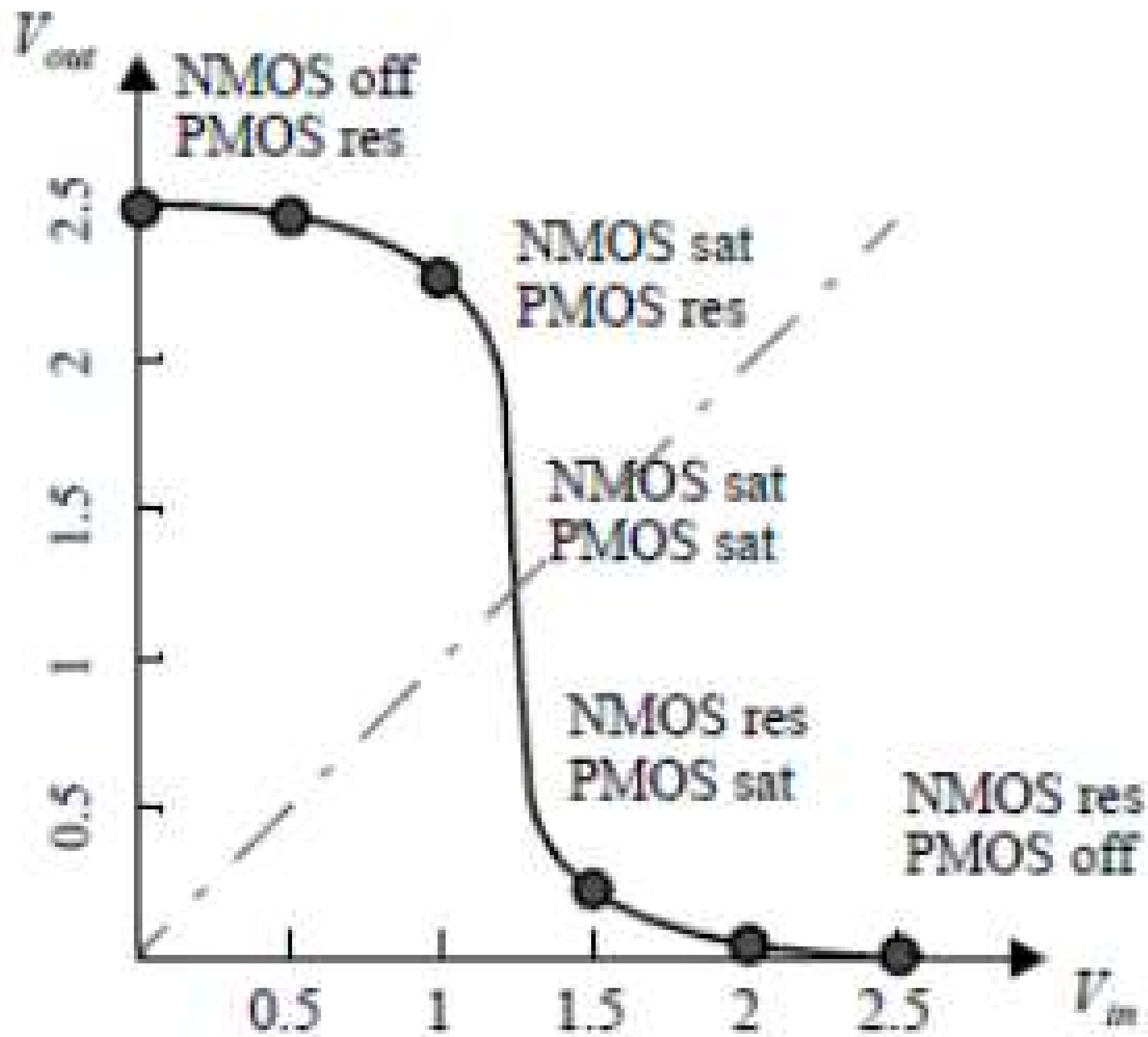


V_{DD}
R_p
Charging
V_{out}
C_L
$V_{in} = 0$
(a) Low-to-high
V_{DD}
V_{out}
C_L
R_n
discharging
$V_{in} = V_{DD}$
(b) High-to-low

DC Characteristics







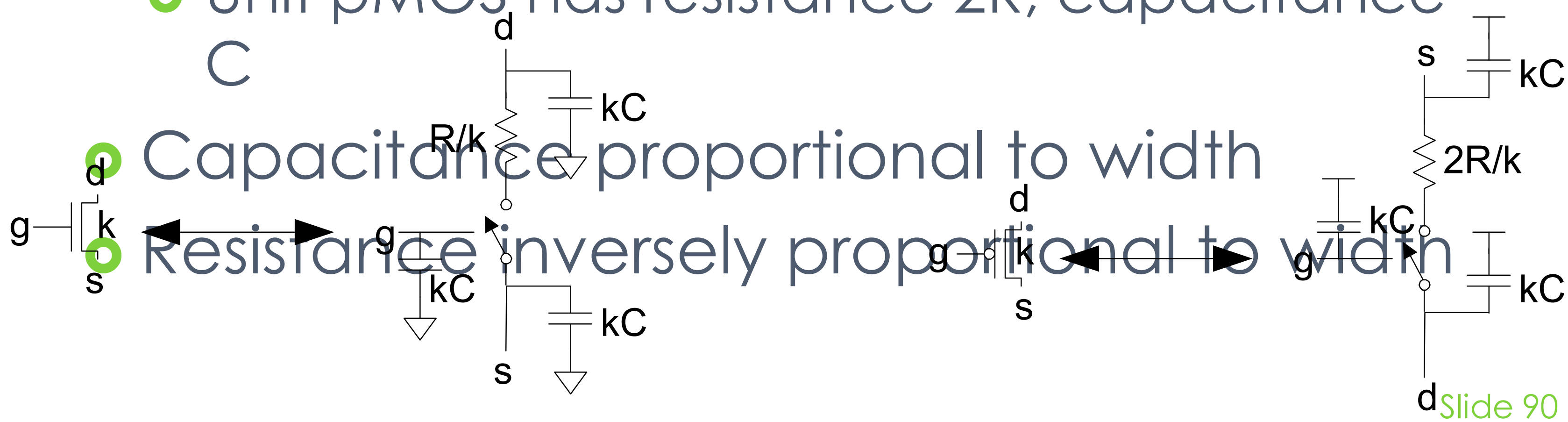
V_{out}
NMOS off
PMOS res
2.5
2
1.5
1
0.5
NMOS sat
PMOS res
NMOS sat
PMOS sat
NMOS res
PMOS sat
NMOS res
PMOS off
0.5
1
1.5
2
2.5
V_{in}

Effective Resistance

- Shockley models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis
- Simplification: treat transistor as resistor
  - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
    - $I_{ds} = V_{ds}/R$
  - R averaged across switching of digital gate
- Too inaccurate to predict current at any given time
  - But good enough to predict delays

RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width

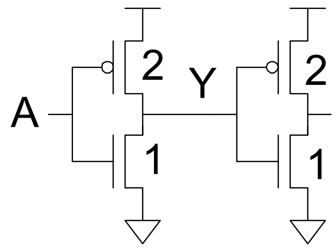


RC Values

- Capacitance
  - $C = C_g = C_s = C_d$ = 2 fF/μm of gate width
  - Values similar across many processes
- Resistance
  - R ≈ 6 KΩ*μm in 0.6um process
  - Improves with shorter channel lengths
- Unit transistors
  - May refer to minimum contacted device (4/2 λ)
  - Or maybe 1 μm wide device
  - Doesn't matter as long as you are consistent

Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



Inverter Delay Estimate

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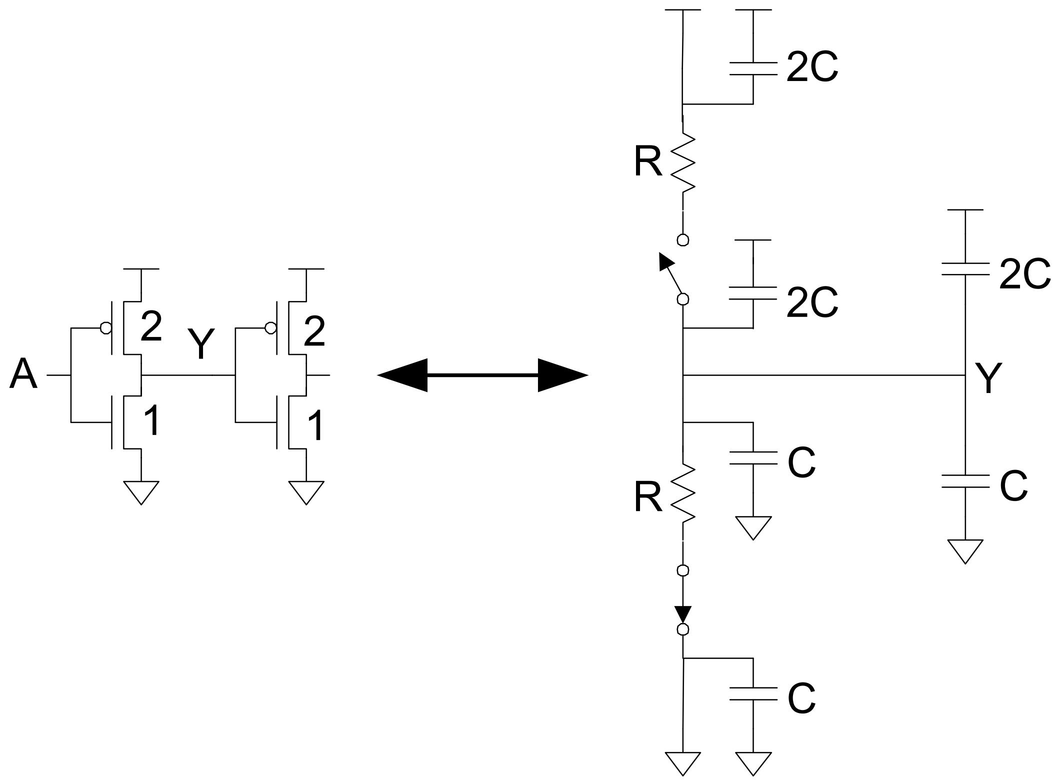

Inverter Delay Estimate

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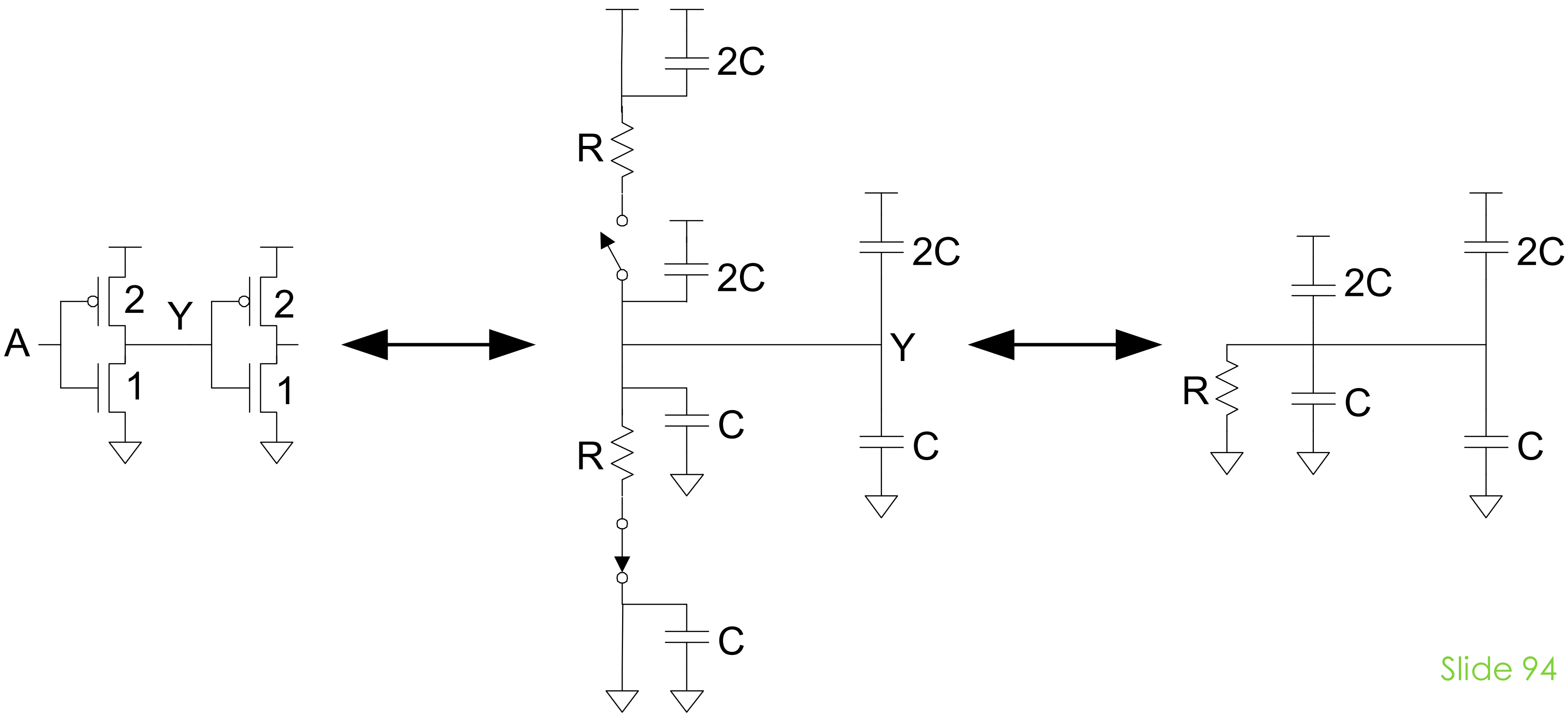
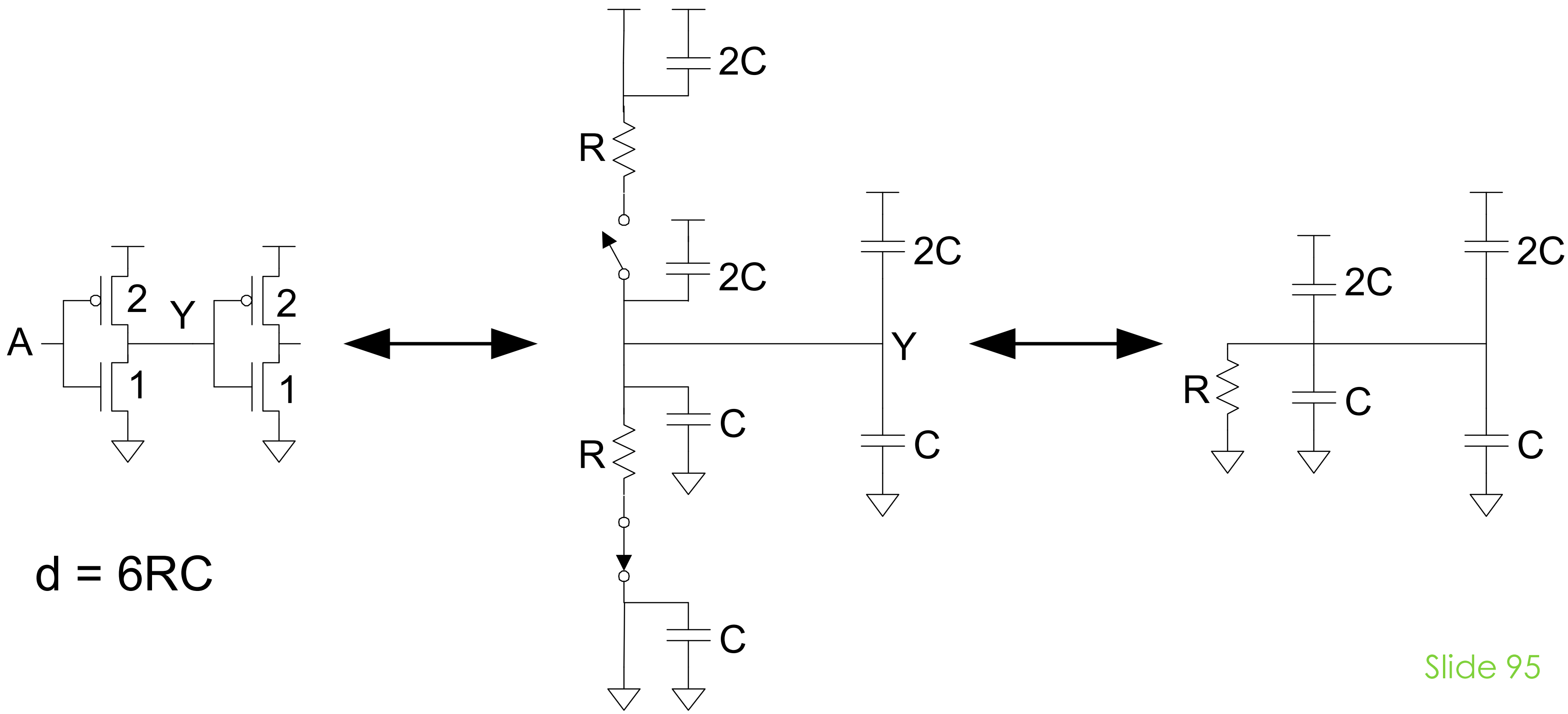


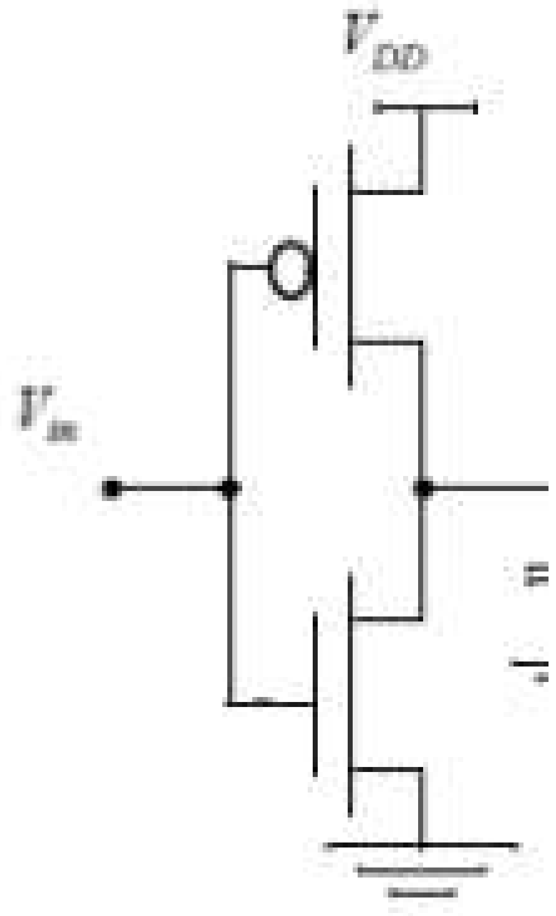
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



d = 6RC

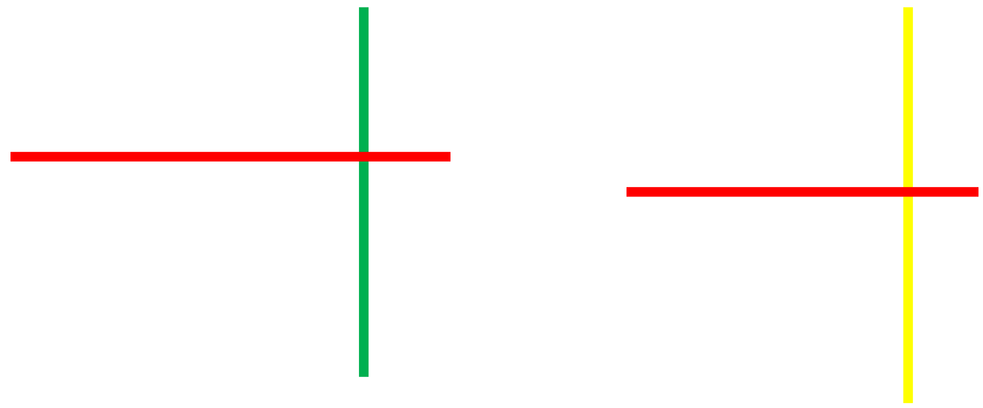
Stick Diagram

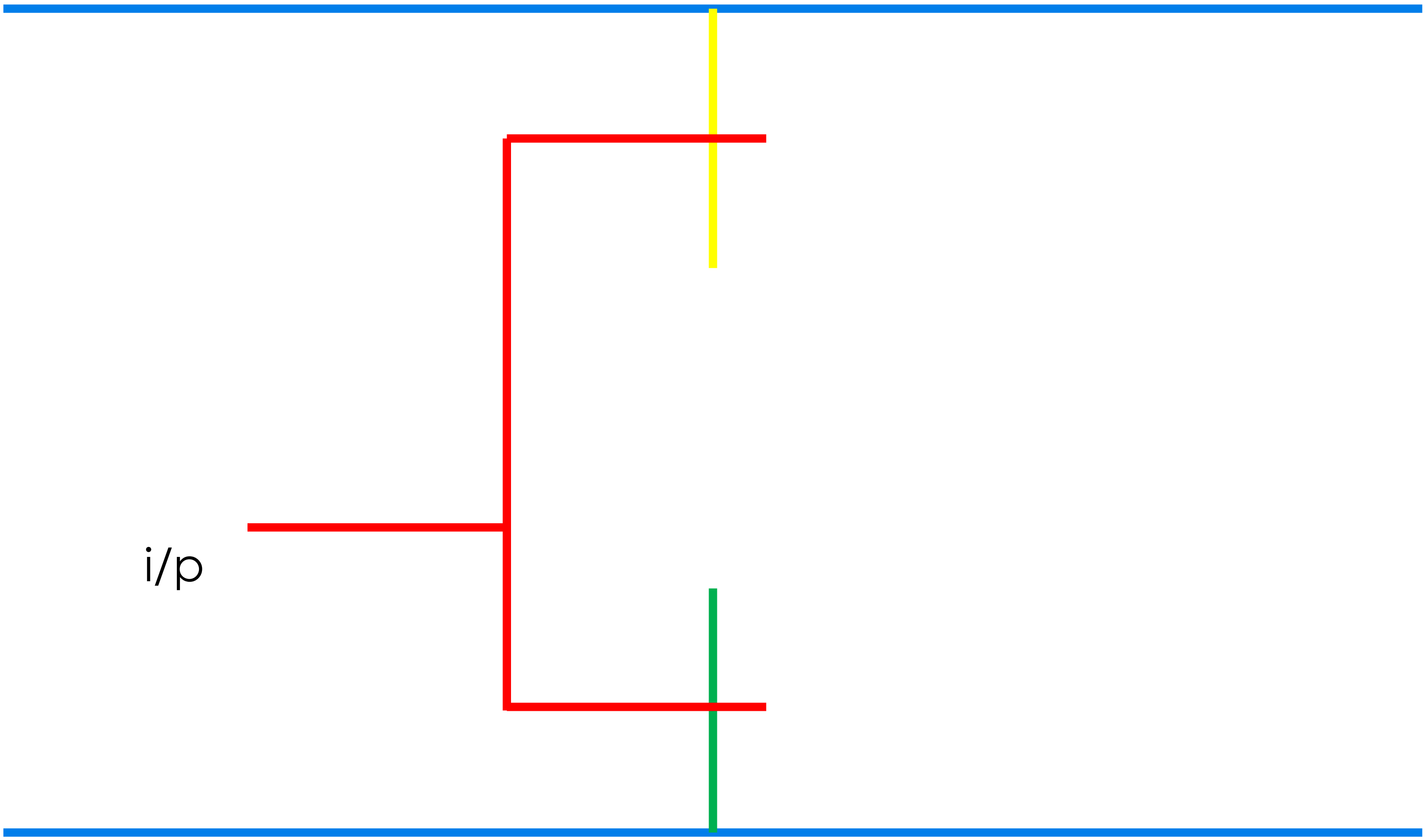


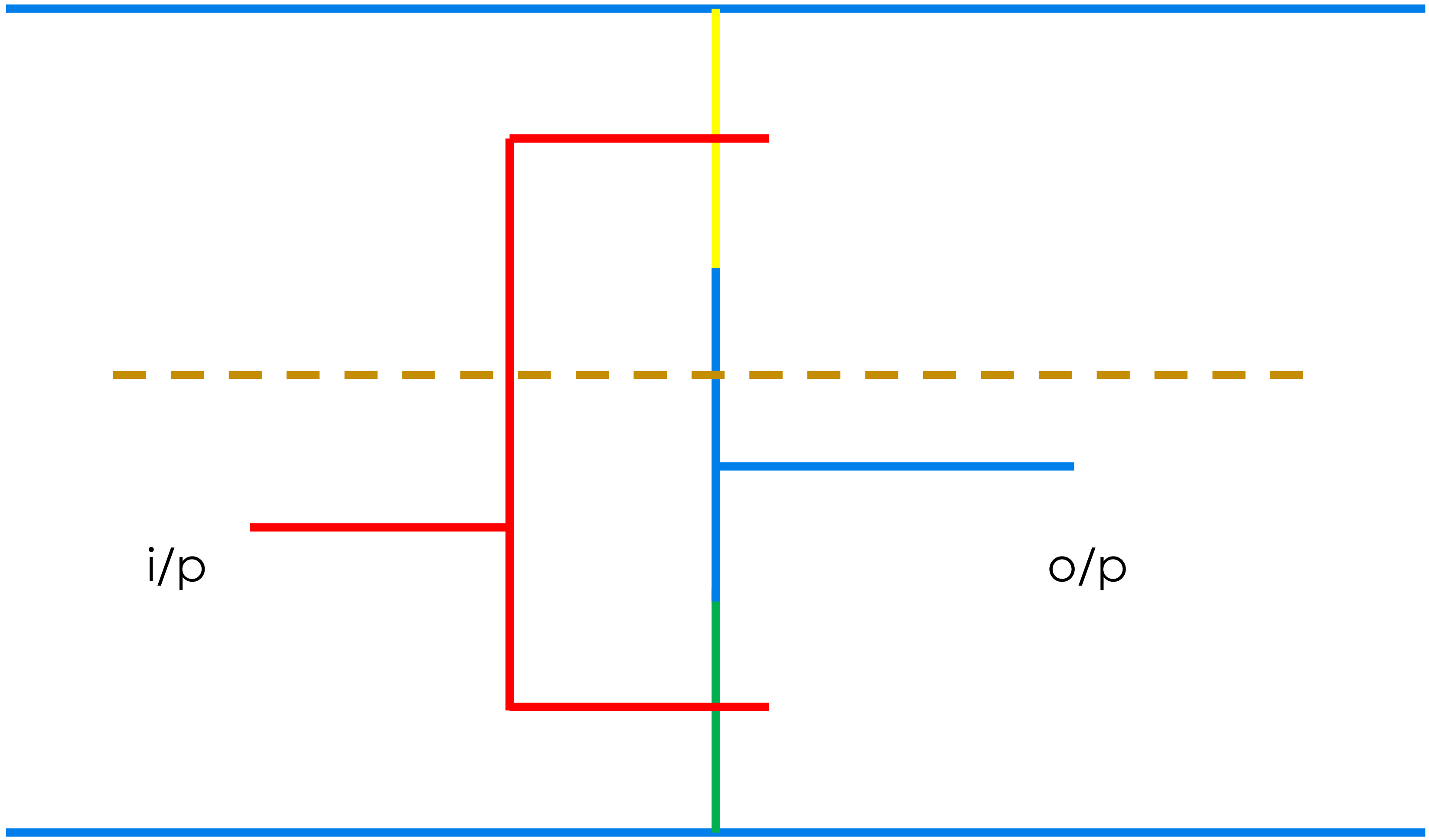
Colour Codes:
Metal – Blue
Polysilicon – Red
N-type – green
P type – yellow
Contacts – black
Demarcation line - brown

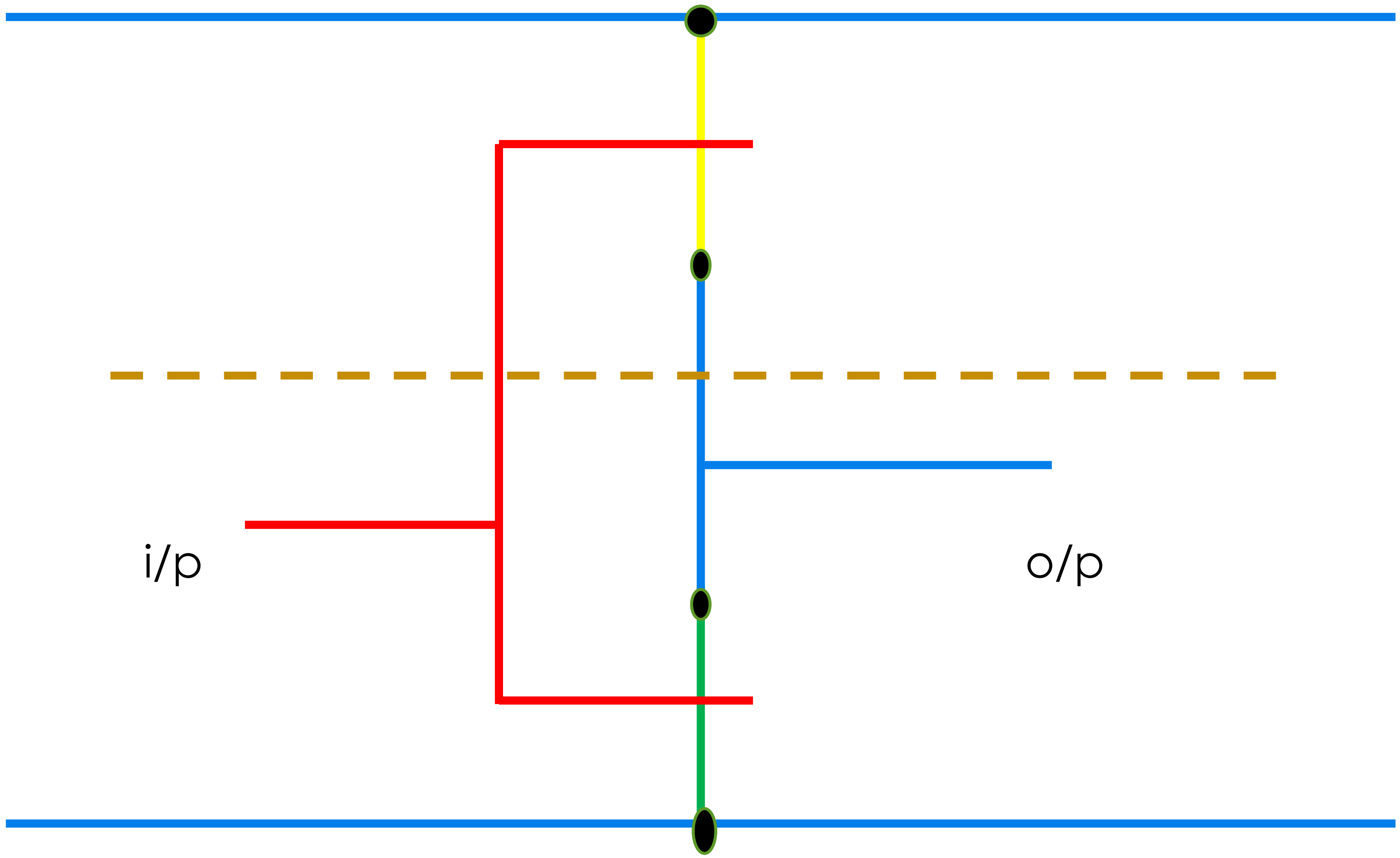
Condition

- Diffusion – Polysilicon –overlap – MOSFET is formed
- No transistor - Diffusion – Polysilicon – should not overlap



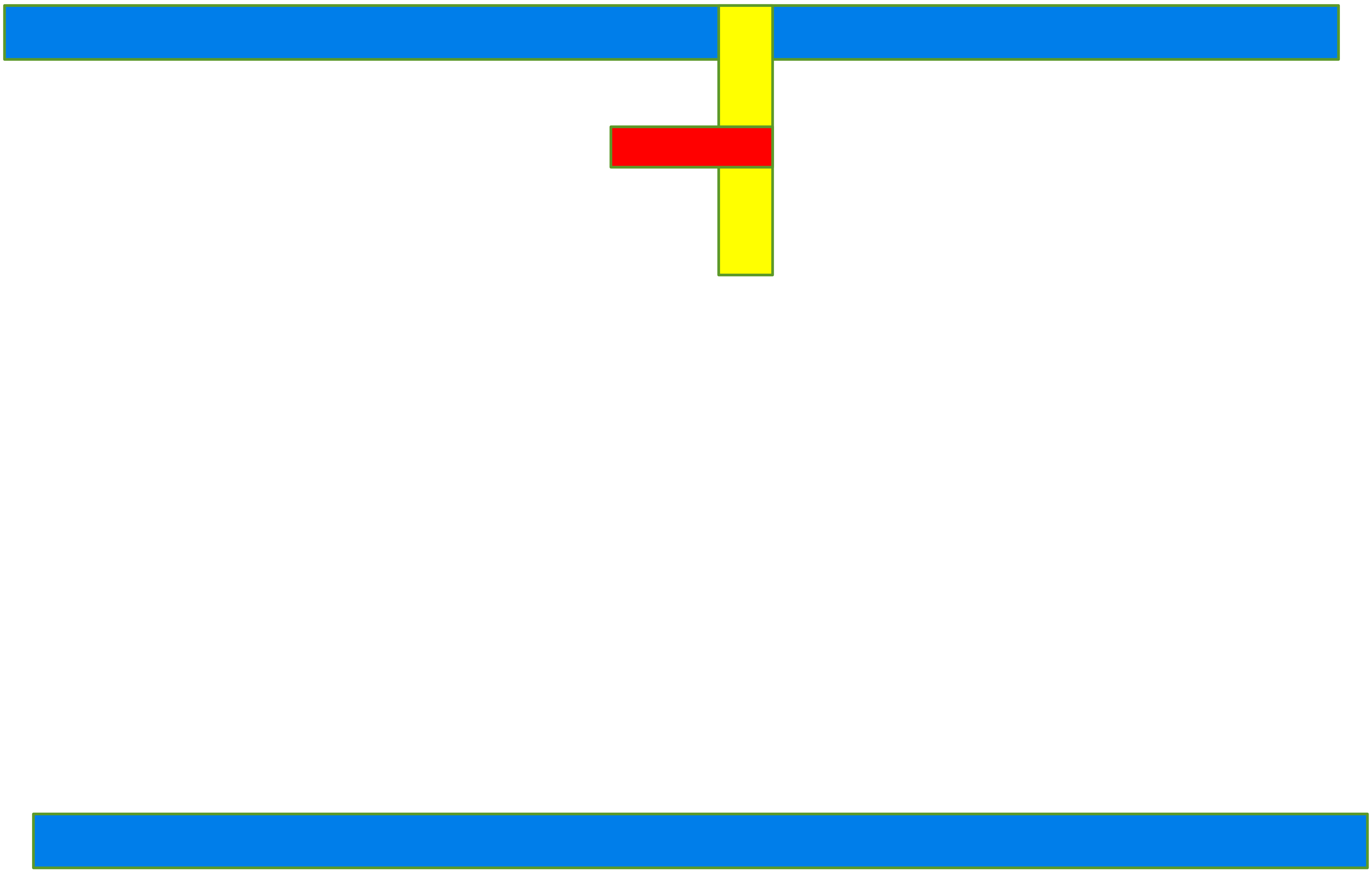

i/p


i/p
o/p

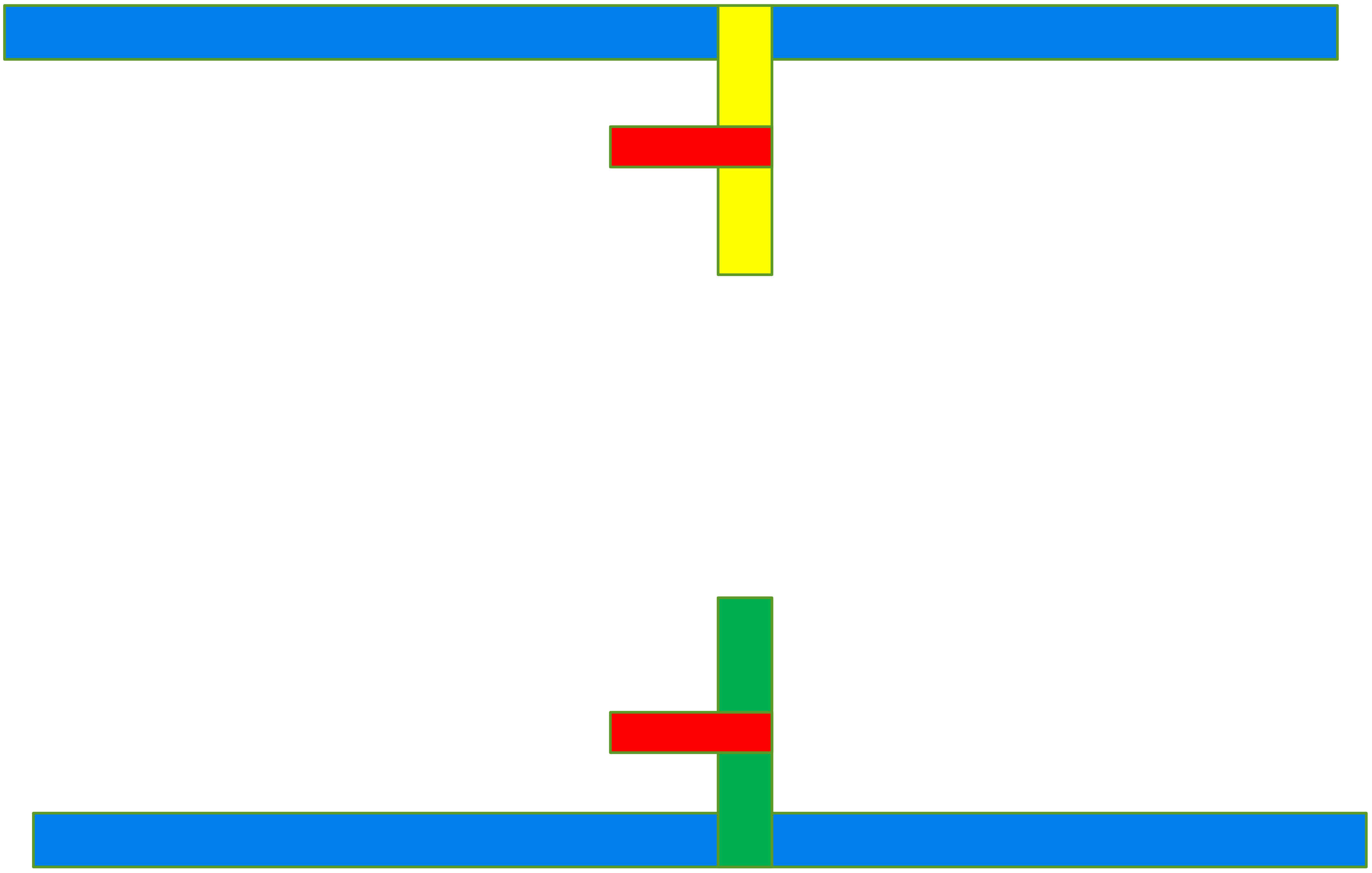

i/p
o/p

- Layout

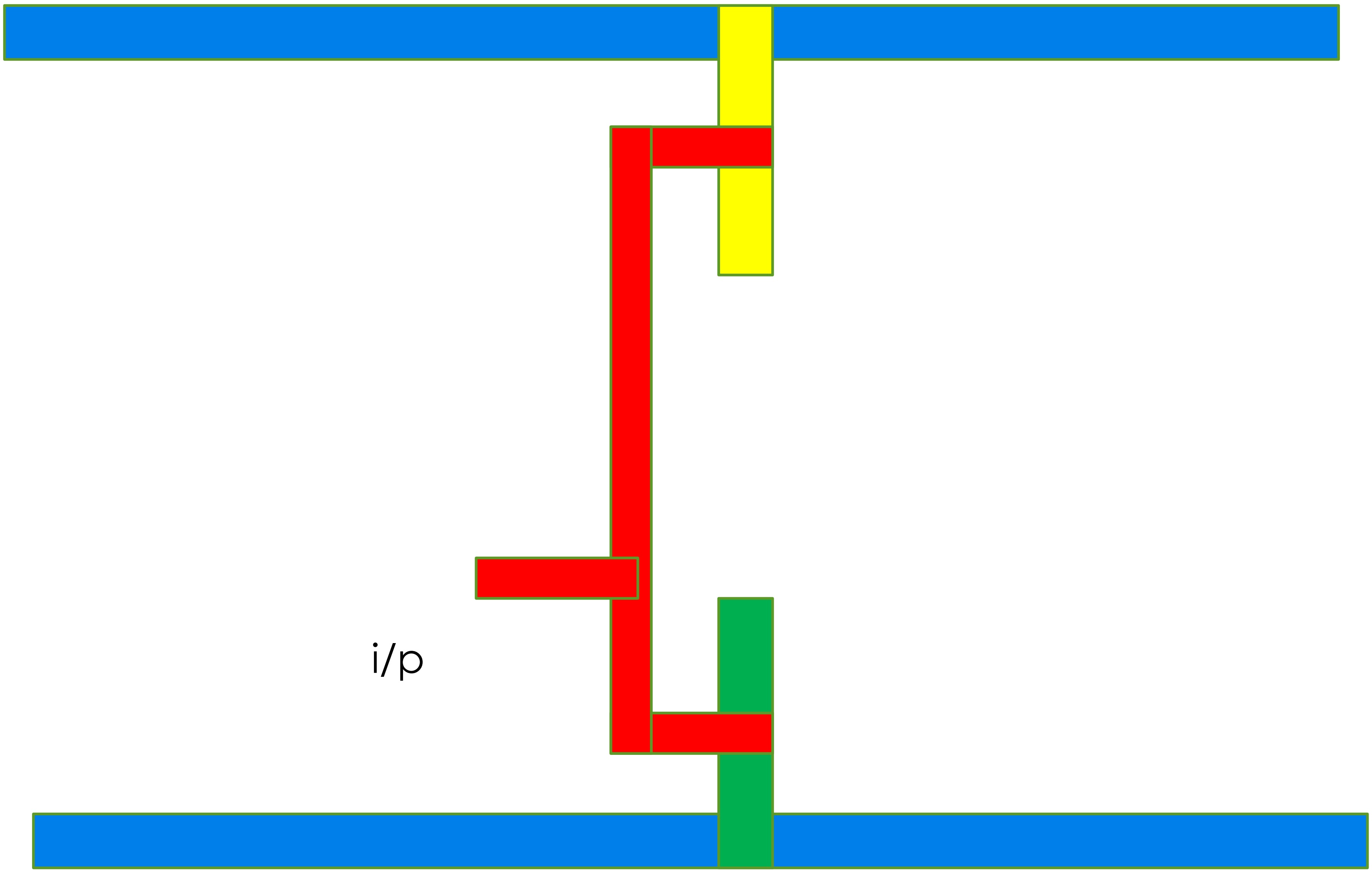
- Layout



- Layout



- Layout



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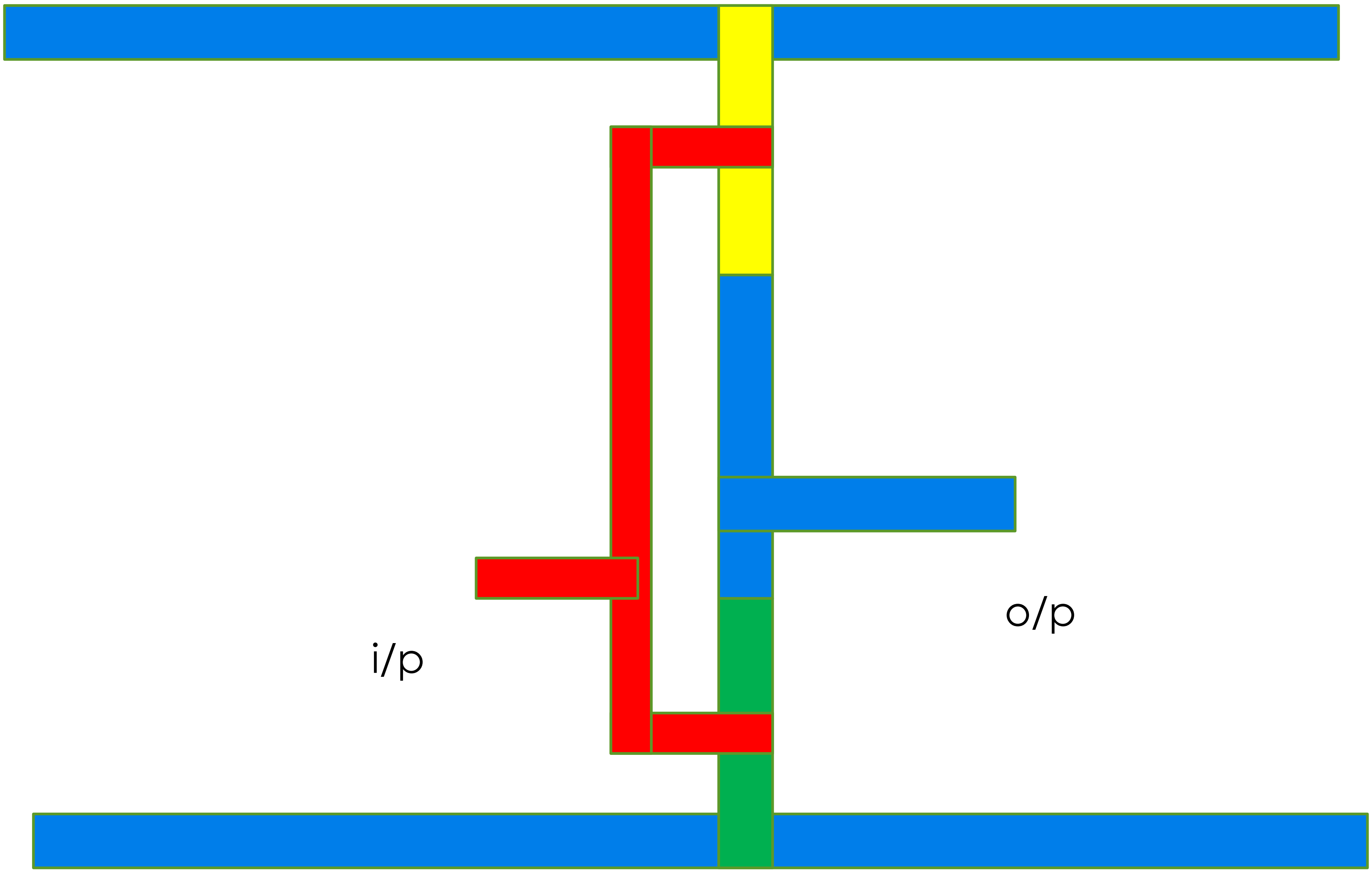

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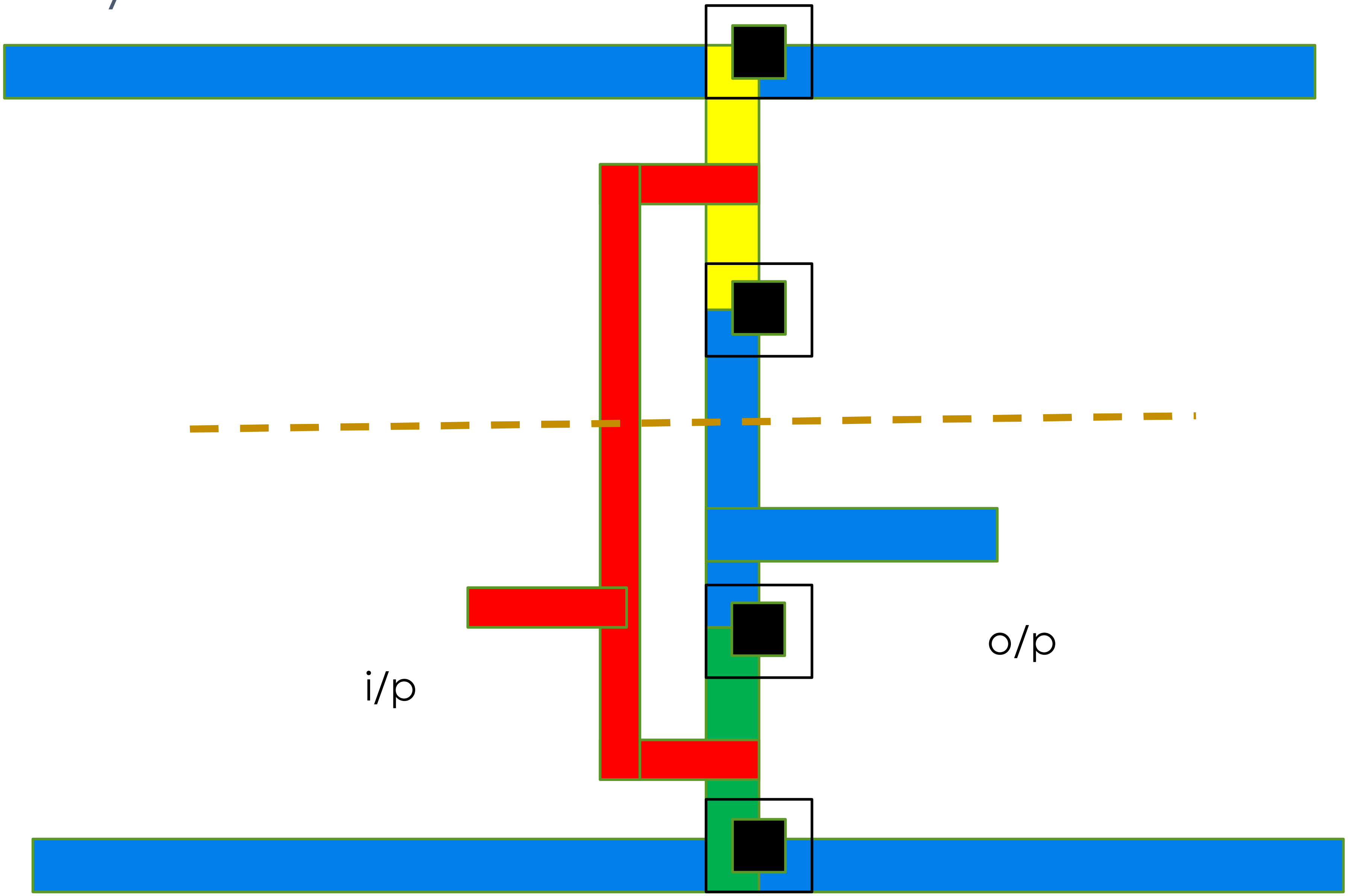
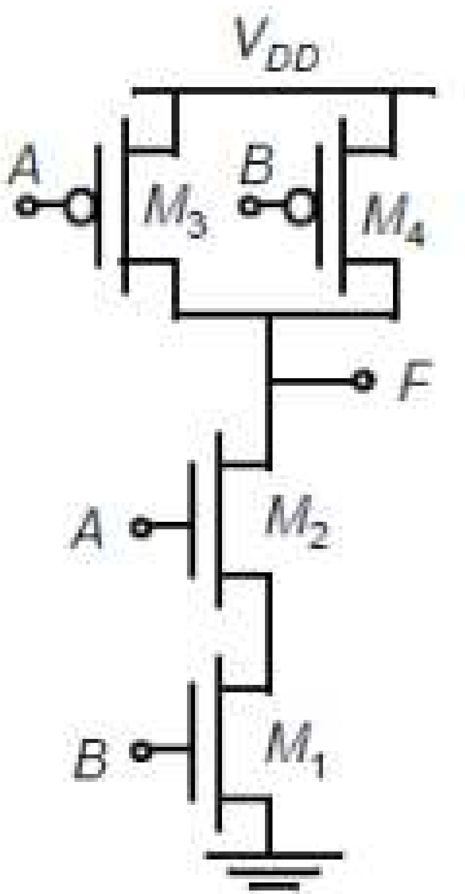
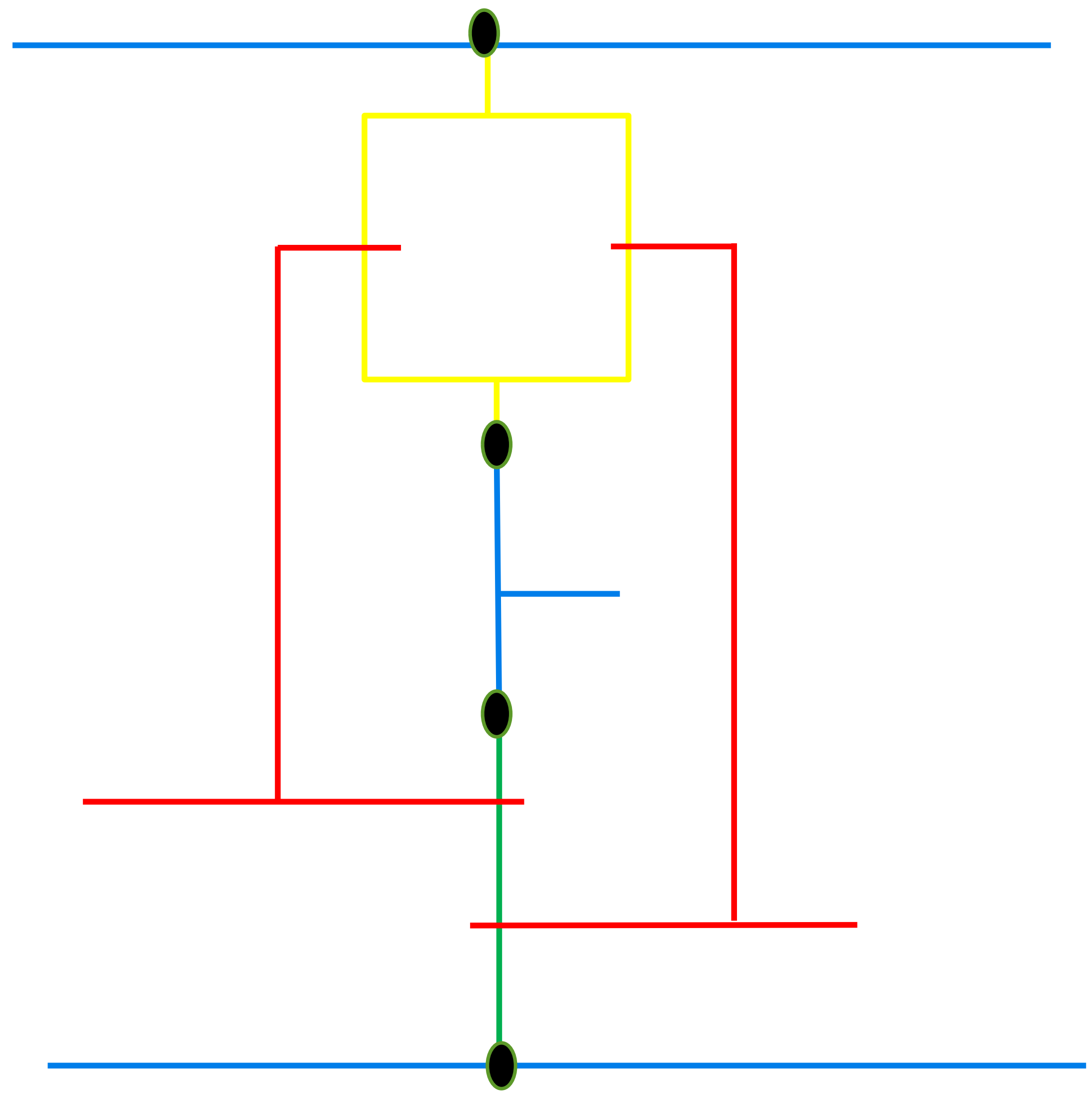
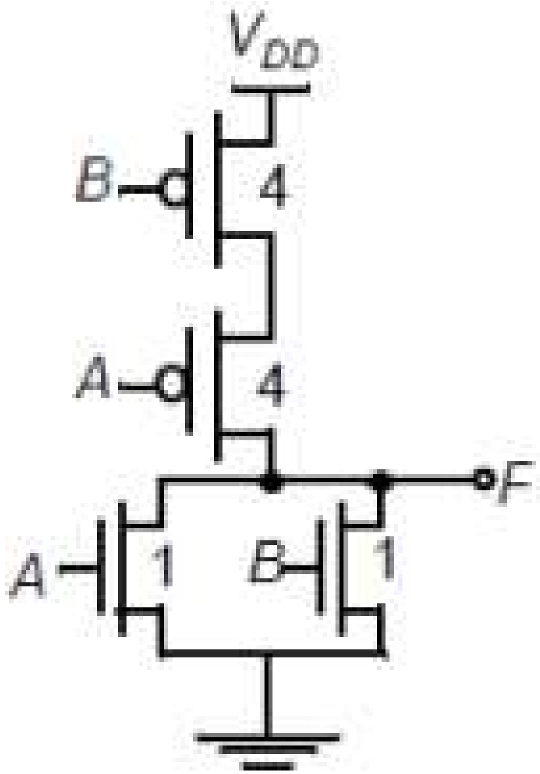


2 input Nand

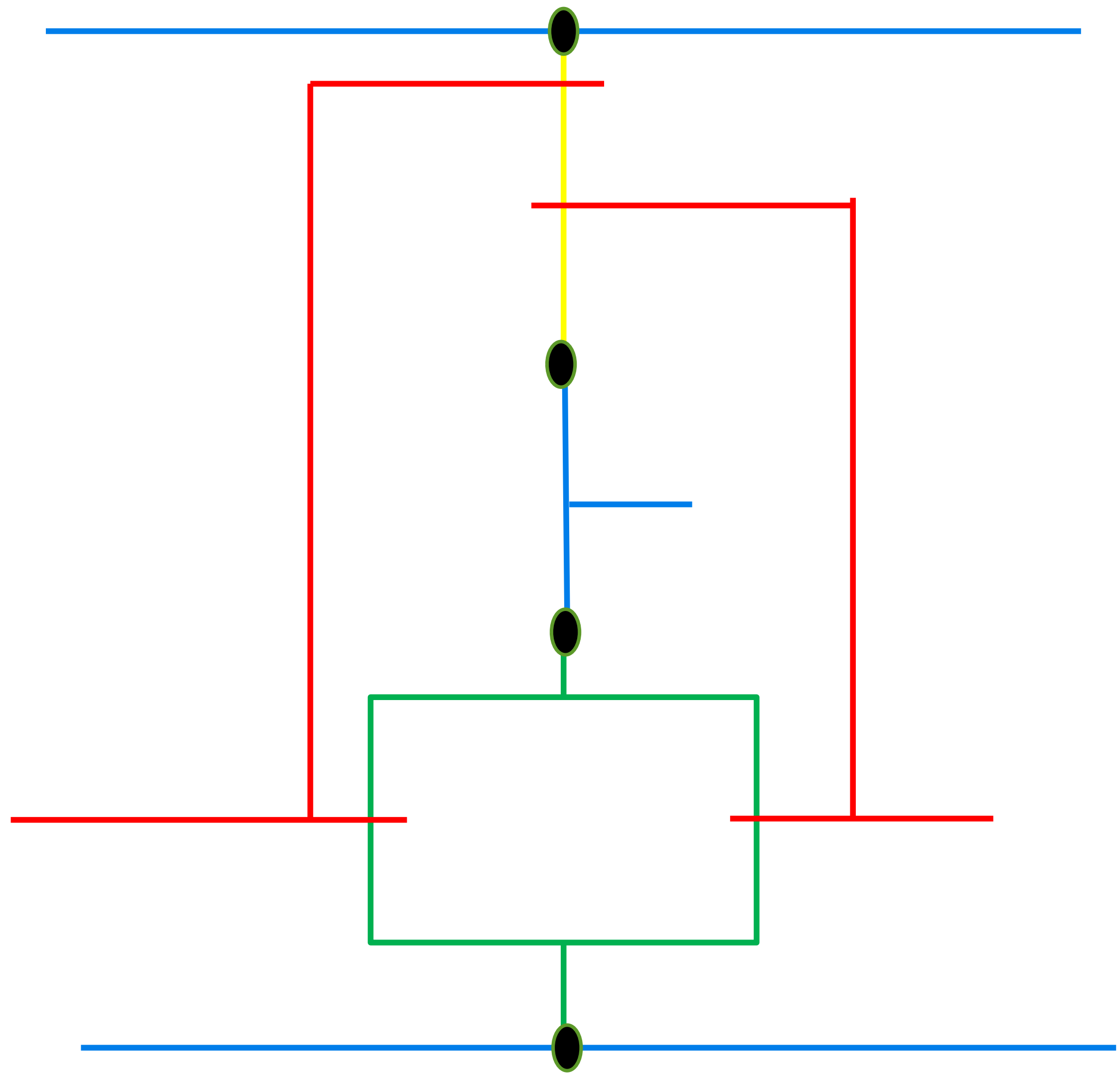




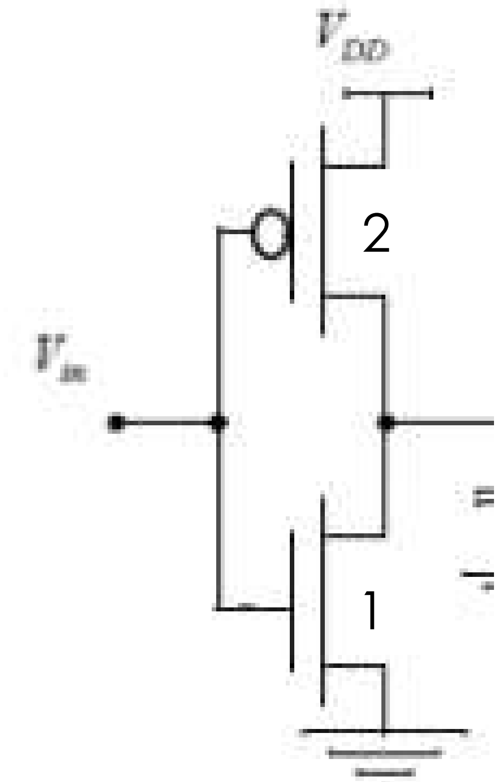
2 input NOR gate

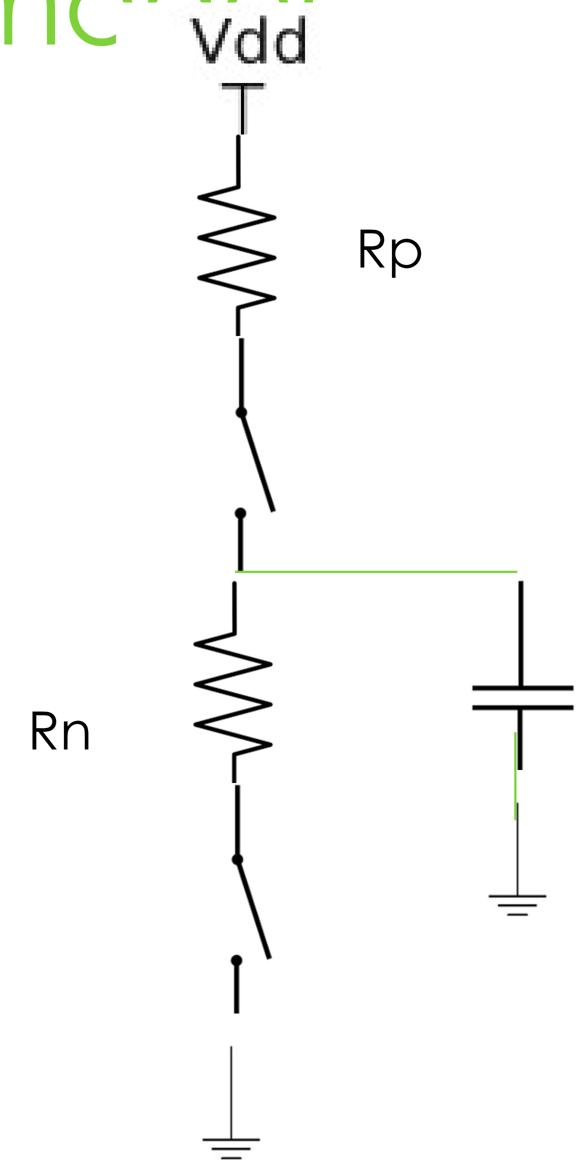


2-input NOR



Elmore delay model

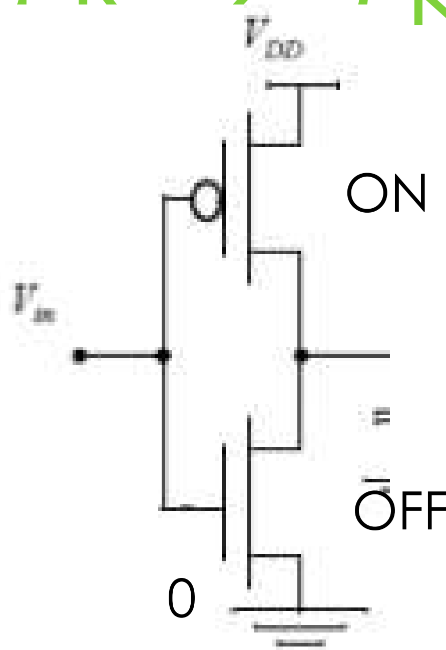


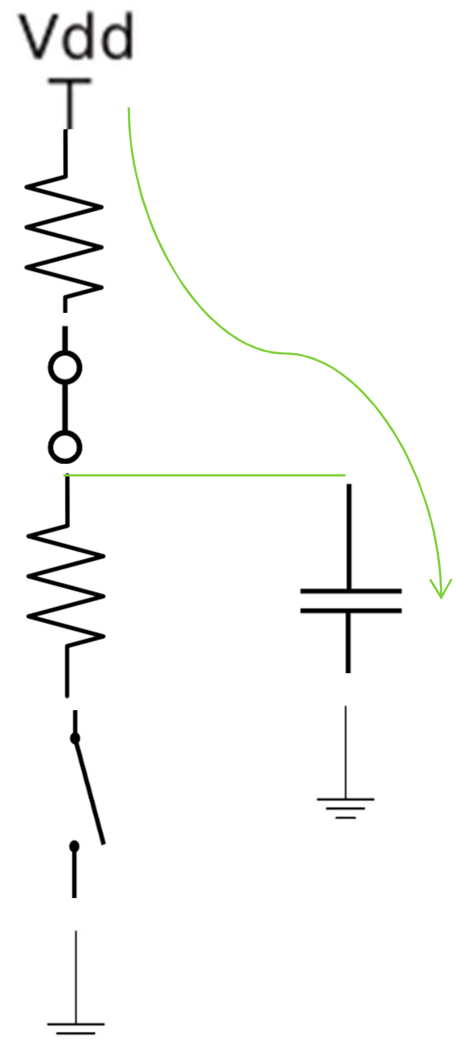


C=2fF/μm and R=2.5 kΩ/μm

A	Y
0	1
1	0

Rising delc

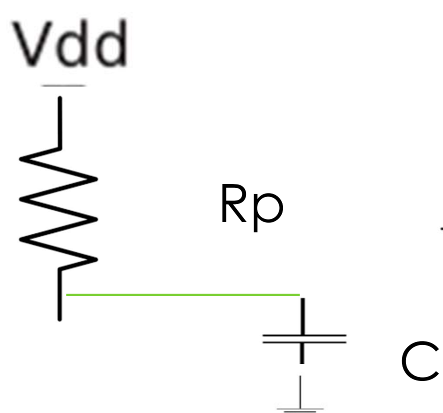




pMOS – G = 0 --- ON – closed switch

nMOS – G = 0 --- OFF --- open switch

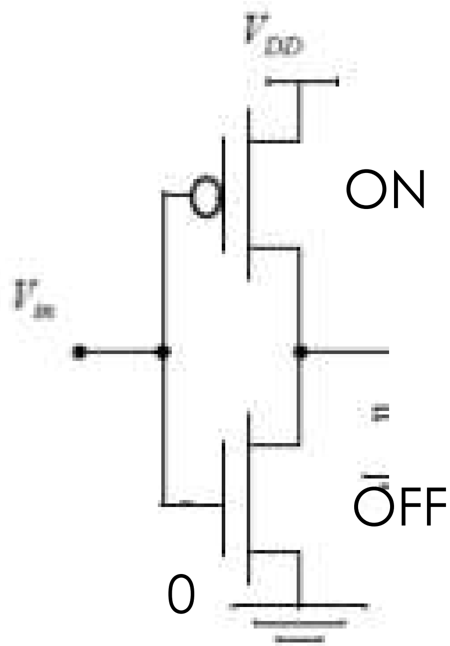
delay = 0.69 R C = 0.69*2.5*2 = 3.45 n sec

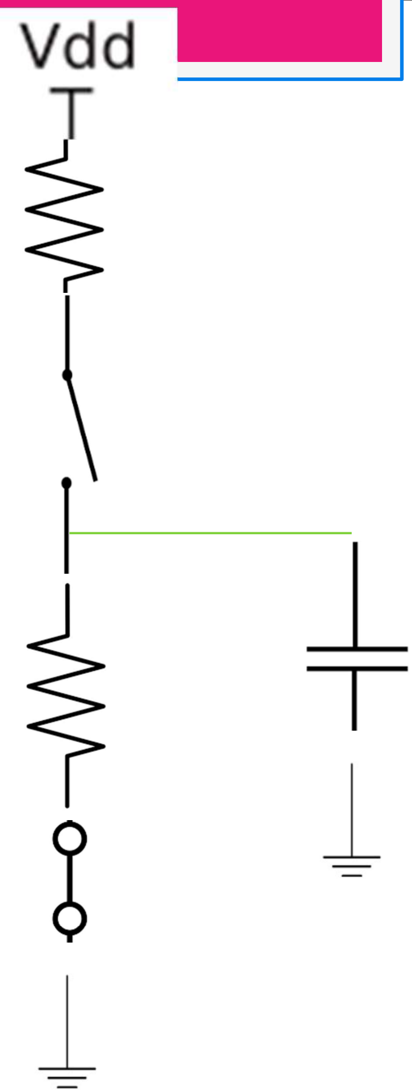


C=2fF/μm and R=2.5 kΩ/μm

A	Y
0	1
1	0

Falling delay



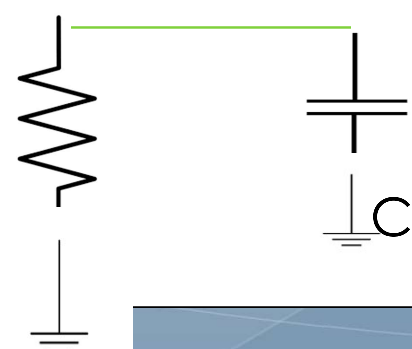


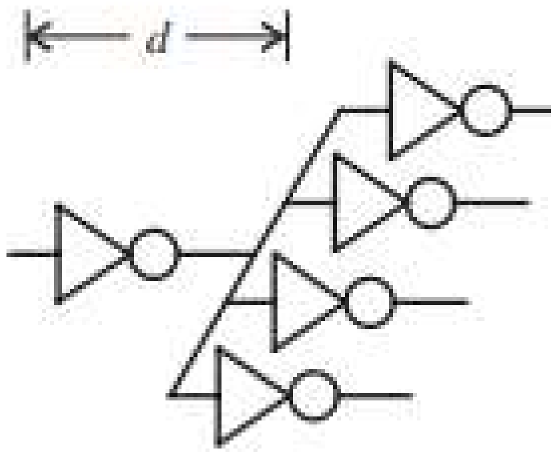
pMOS – G = 1 --- OFF – open switch

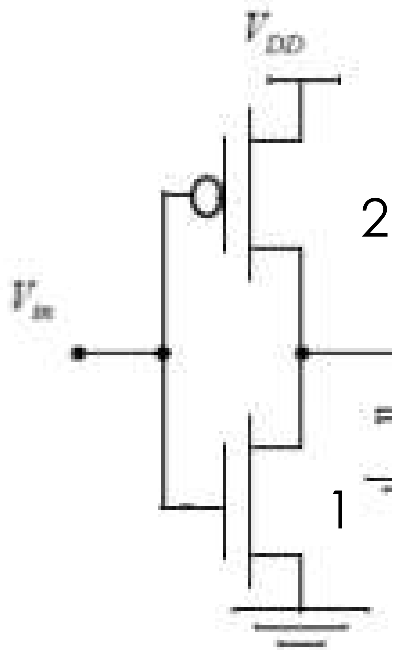
nMOS – G = 1 --- ON --- closed switch

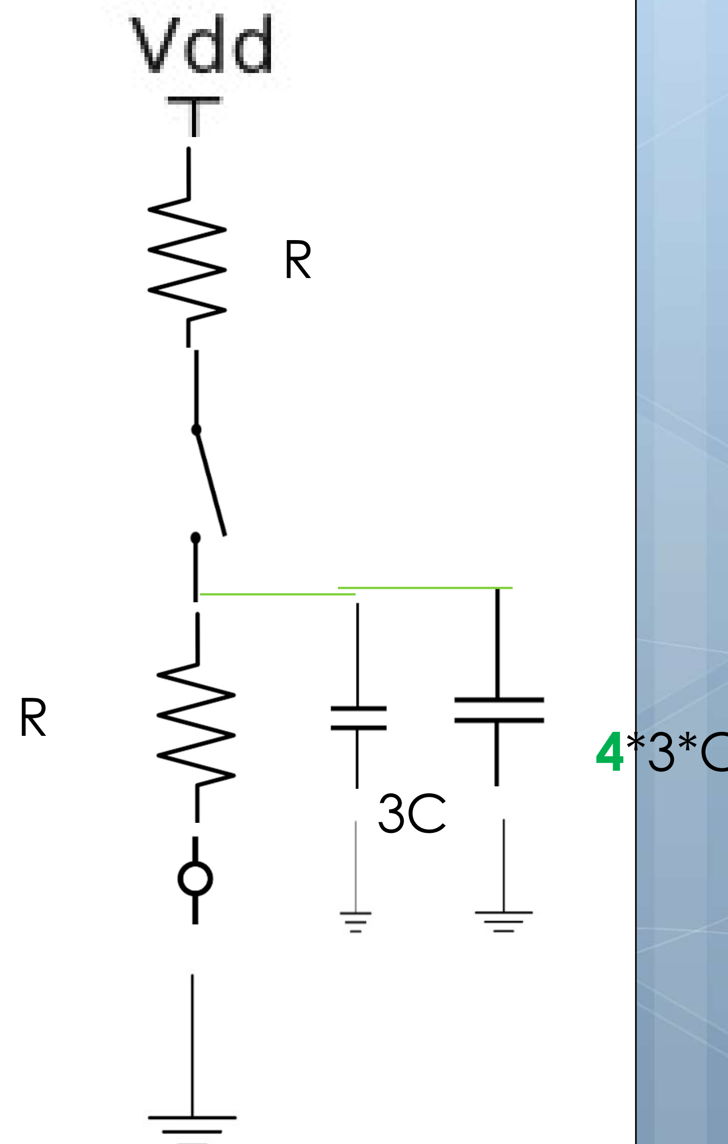
delay = 0.69 R C = 0.69*2.5*2 = 3.45nsec

Rn









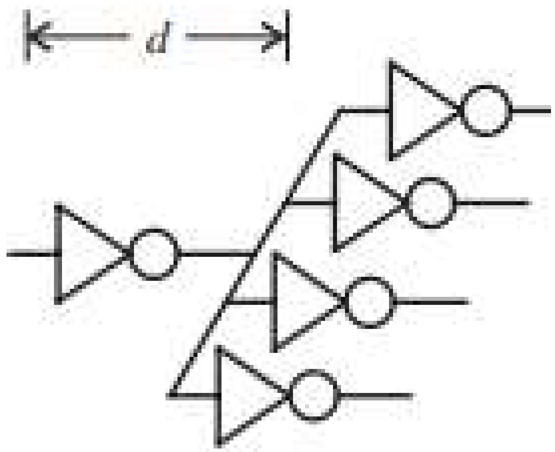
A	Y
0	1
1	0

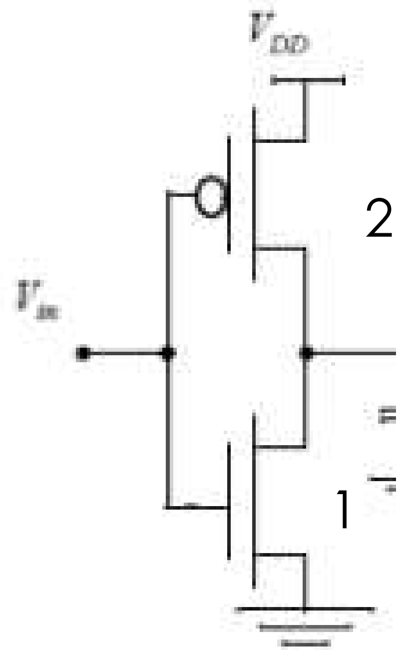
i/p=1 , Falling delay

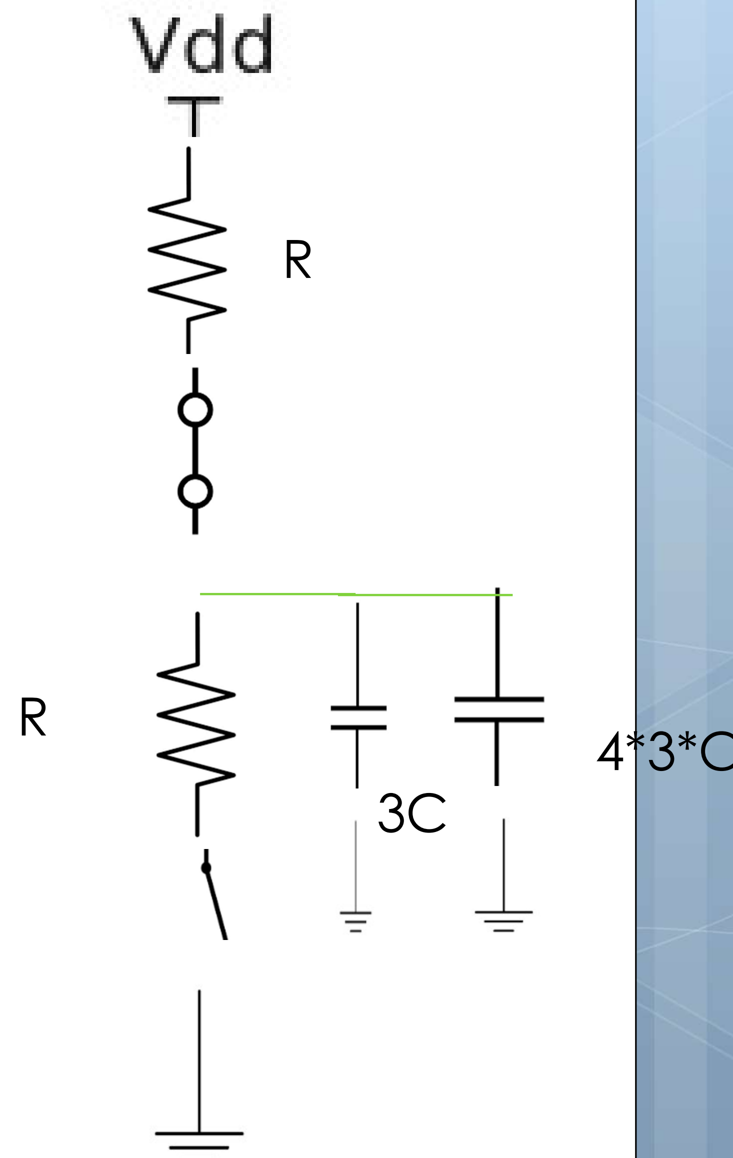
nMos—G=1 –ON – Closed switch

pMos ---G=1, OFF – Open switch

D = 0.69 R (3+12)C = 0.69* 2.5K*15*2f =







A	Y
0	1
1	0

i/p=0 , Rising delay

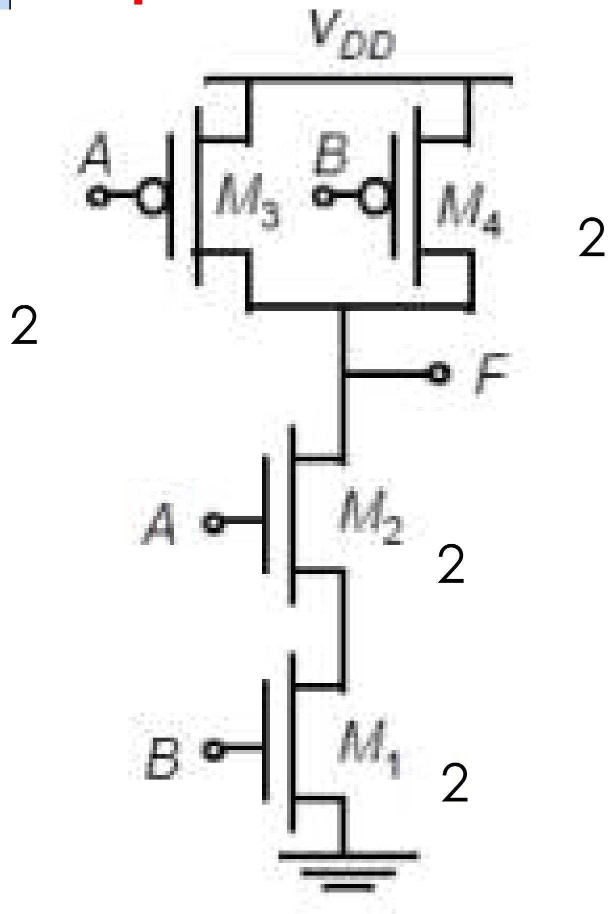
nMos—G=0 –OFF – open switch

pMos ---G=0, ON – Closed switch

D = 0.69 R (3+12)C = 0.69* 2.5K*15*2f =

- Sketch a 2 input NAND gate with transistor width chosen to achieve effective rise and fall resistance equal to the unit inverter.
- Compute the rising and falling propagation delay (in terms of R and C) of the NAND gate driving **h identical NAND gates** using the Elmore delay model.
- If C=2fF/μm and R=2.5 kΩ/μm in a 180nm process what is the delay of a fanout of 3 NAND gate

2 input NAND gate



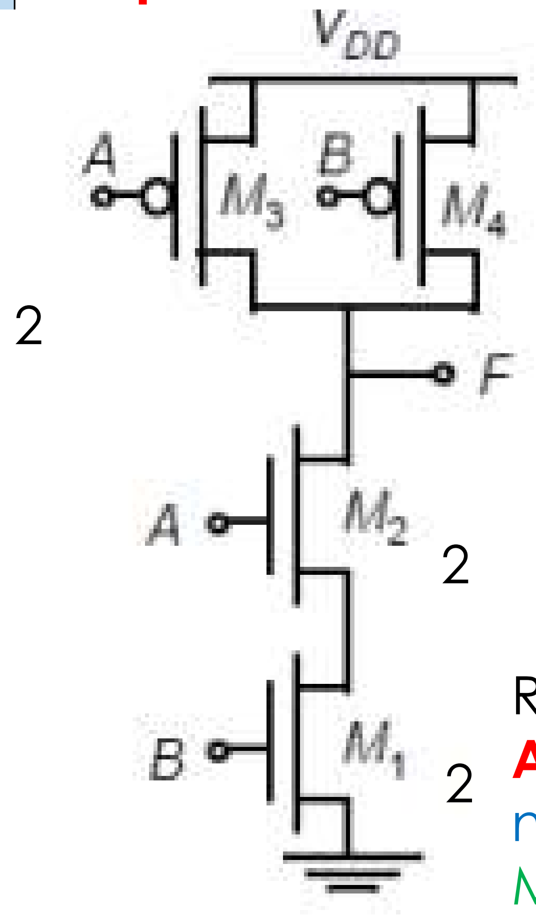
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Rising delay

Falling delay

Falling delay
A=1,B=1
nMOS – Gate =1 – On – Closed switch
M1, M2 – On - Closed switch
pMOS – Gate =1 – Off – open switch
M3, M4 – On - open switch

2 input NAND gate



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Rising delay

Falling delay

Rising delay

A=1,B=0

nMOS – Gate =1 – On – Closed switch

M1, B = 0 Gate=0 – [Off -- open switch]

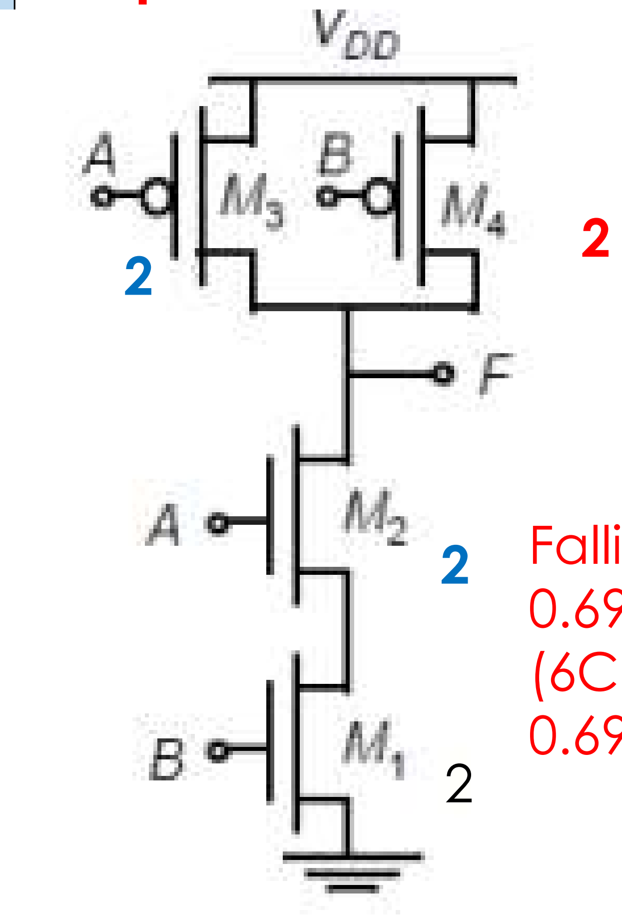
M2 – A=1, Gate= 1– (On - Closed switch)

pMOS – Gate =0 – On – Closed switch

M3 – A= 1, Gate= 1- (Off – Open switch)

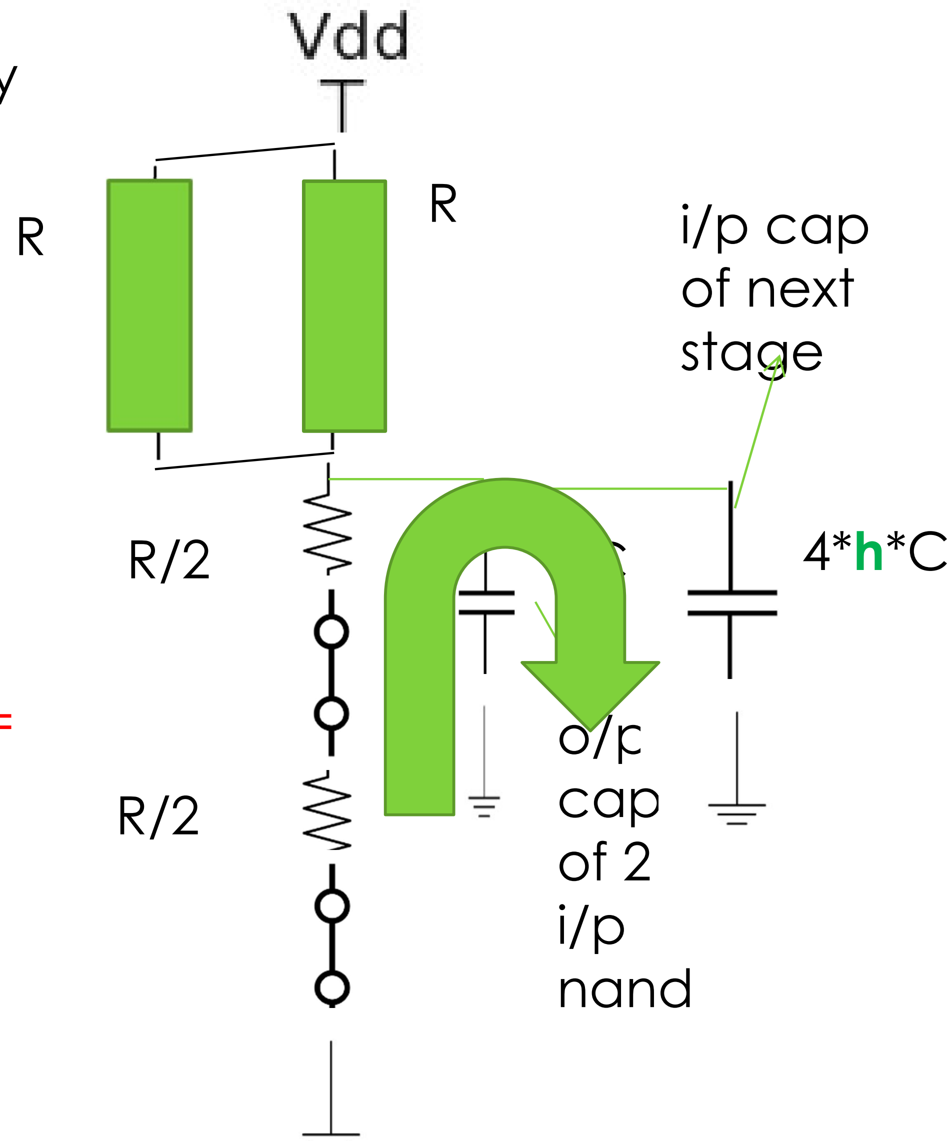
M4 – B=0, Gate =0 – [On – Closed switch]

2 input NAND gate



Falling delay

Falling delay = 0.69 * (R/2+R/2)* (6C+4hC) = 0.69*R* C(6+4h) =

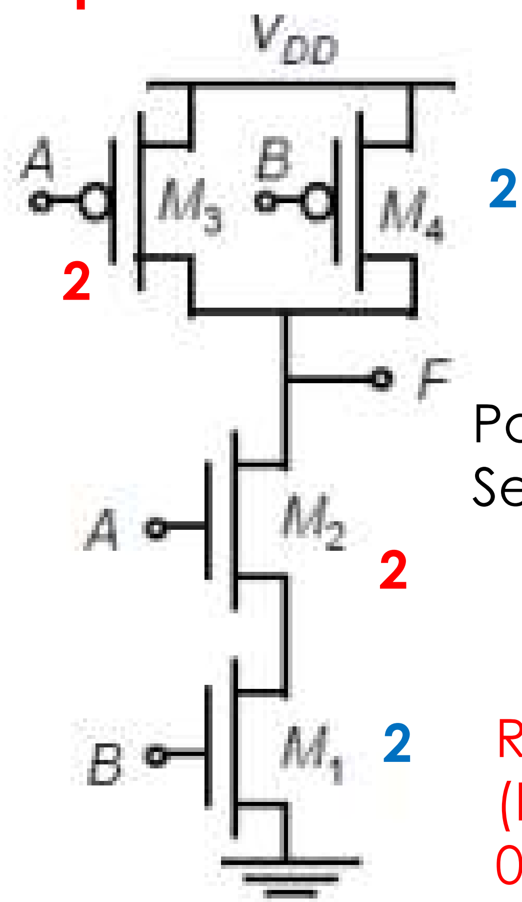


Parallel resistor – R
Series resistor – R/n

Falling delay
A=1,B=1

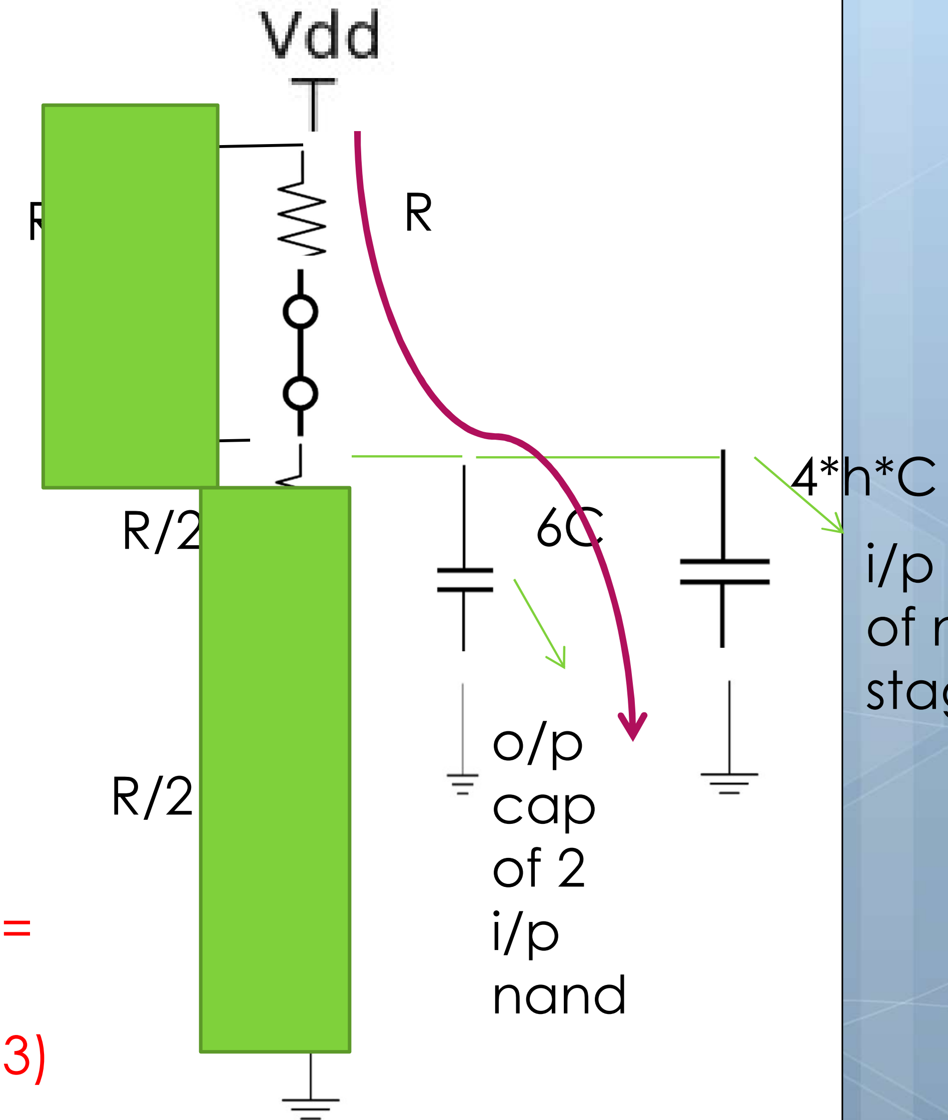
nMOS – Gate =1 – On – Closed switch == M1, M2 – On - Closed switch
pMOS – Gate =1 – Off – open switch == M3, M4 – On - open switch

2 input NAND gate



Parallel resistor – R
Series resistor – R/n

Rising delay = 0.69 * (R)* (6C+4hC) = 0.69*R* C(6+4h) = 0.69*2.5k*2fF*(6+4h) = assume h=3
= 0.69*2.5k*2fF*(6+4*3)

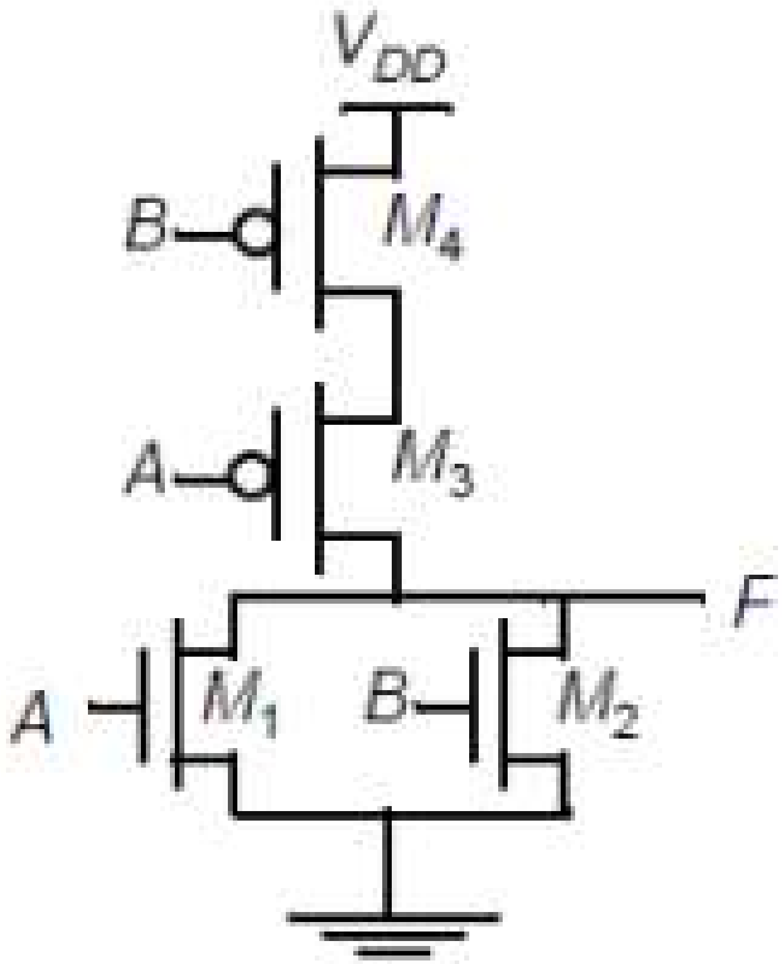


Rising delay

A=1,B=0

nMOS – Gate =1 – On – Closed switch

- Consider the 2 input NOR gate of Figure .
- Assume NMOS and PMOS devices of 0.5mm/0.25mm and 0.75mm/0.25mm, respectively.
- This sizing should result in approximately equal worst-case rise and fall times (since the effective resistance of the pull-down is designed to be equal to the pull-up resistance).



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Rising delay

Falling del

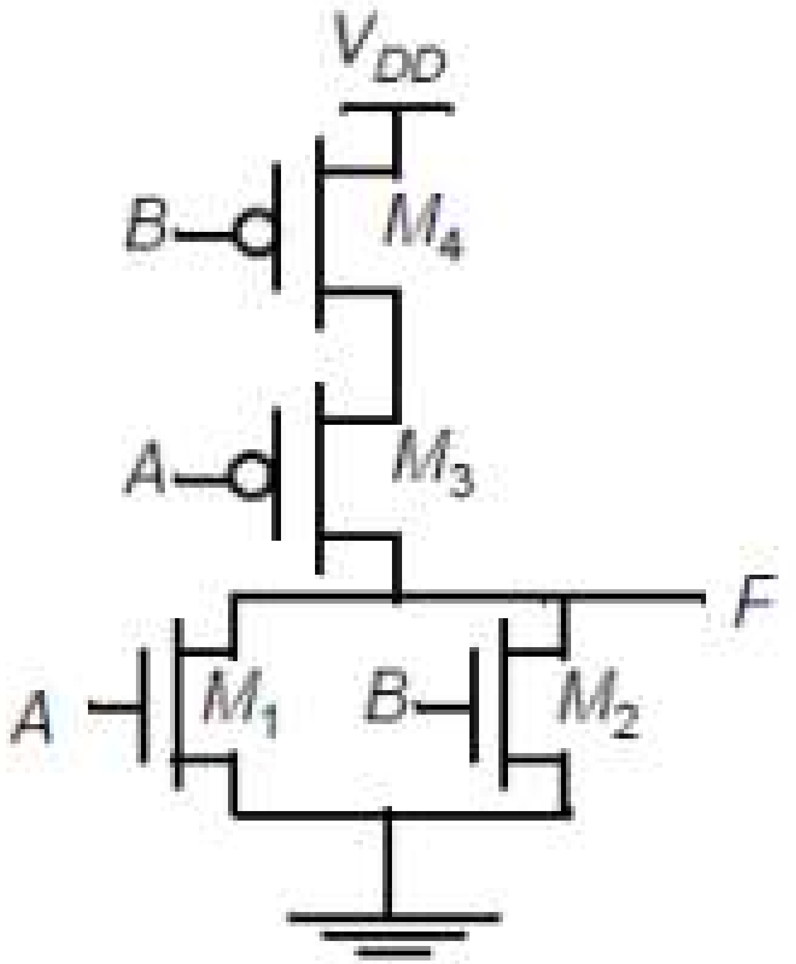
Rising delay

nMOS – gate =1 –on – closed switch

A=0 B=0

M1,M2 – Off – open switch

M3,M4 – On – Closed switch



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Rising delay

Falling del

Falling delay

nMOS – gate =1 –on – closed switch

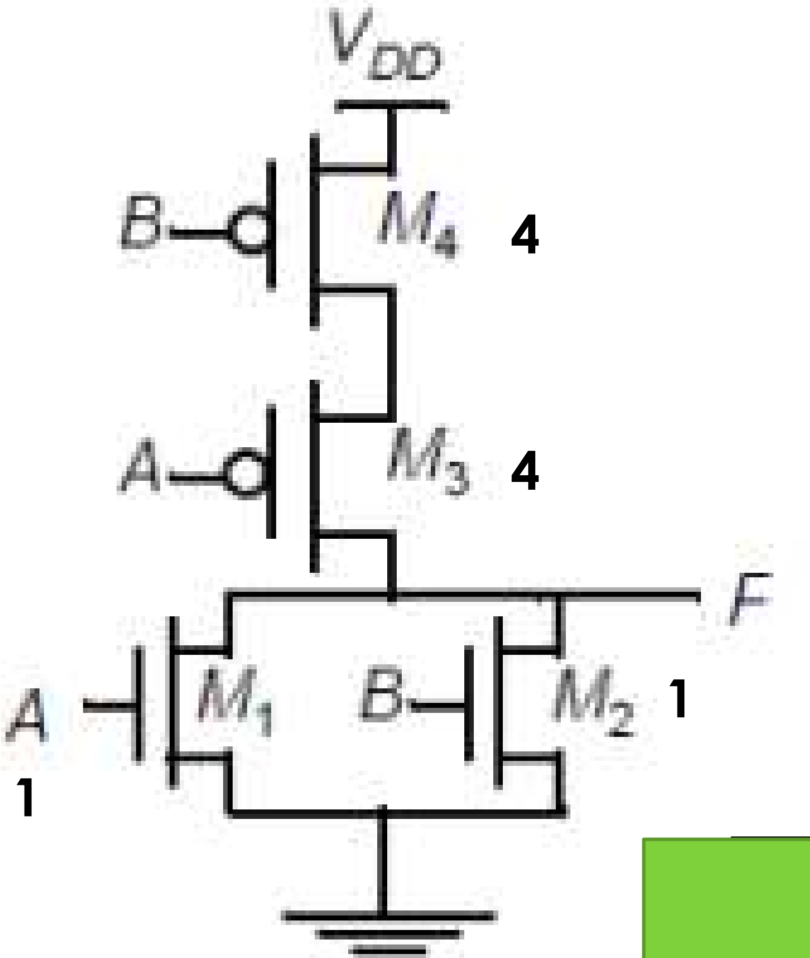
A=0 B=1

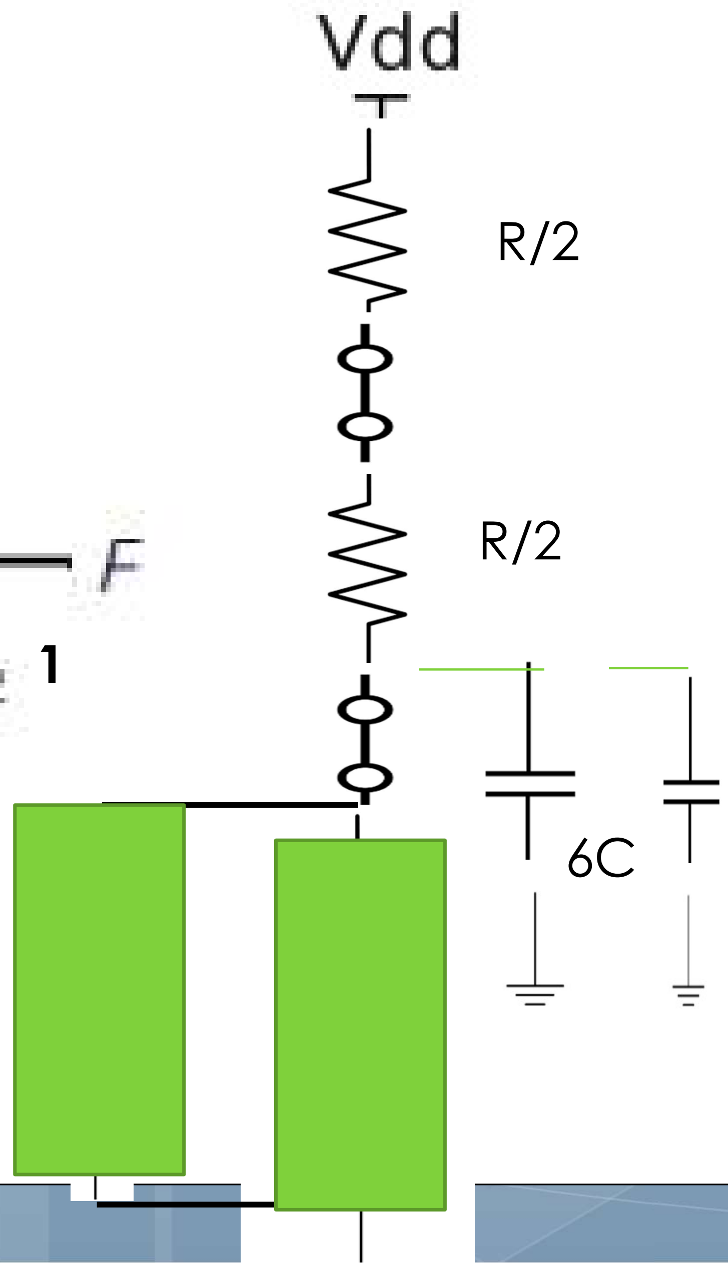
M1,- Off – open switch

M3,- On – Closed switch

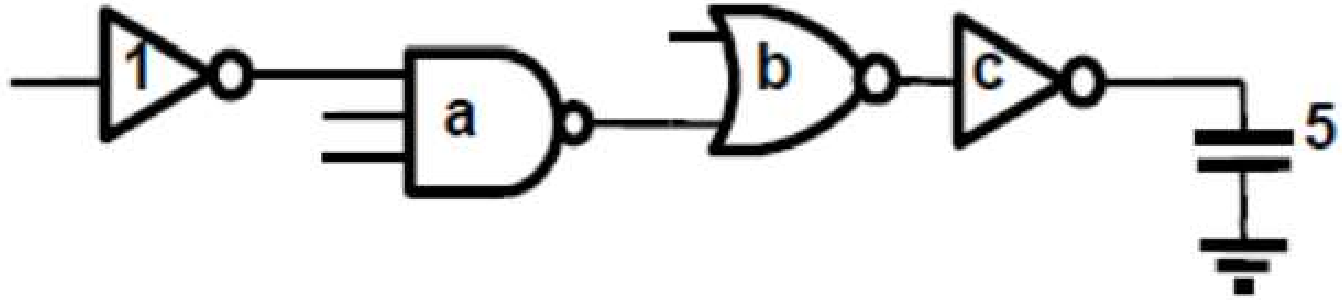
M2 – On – Closed switch

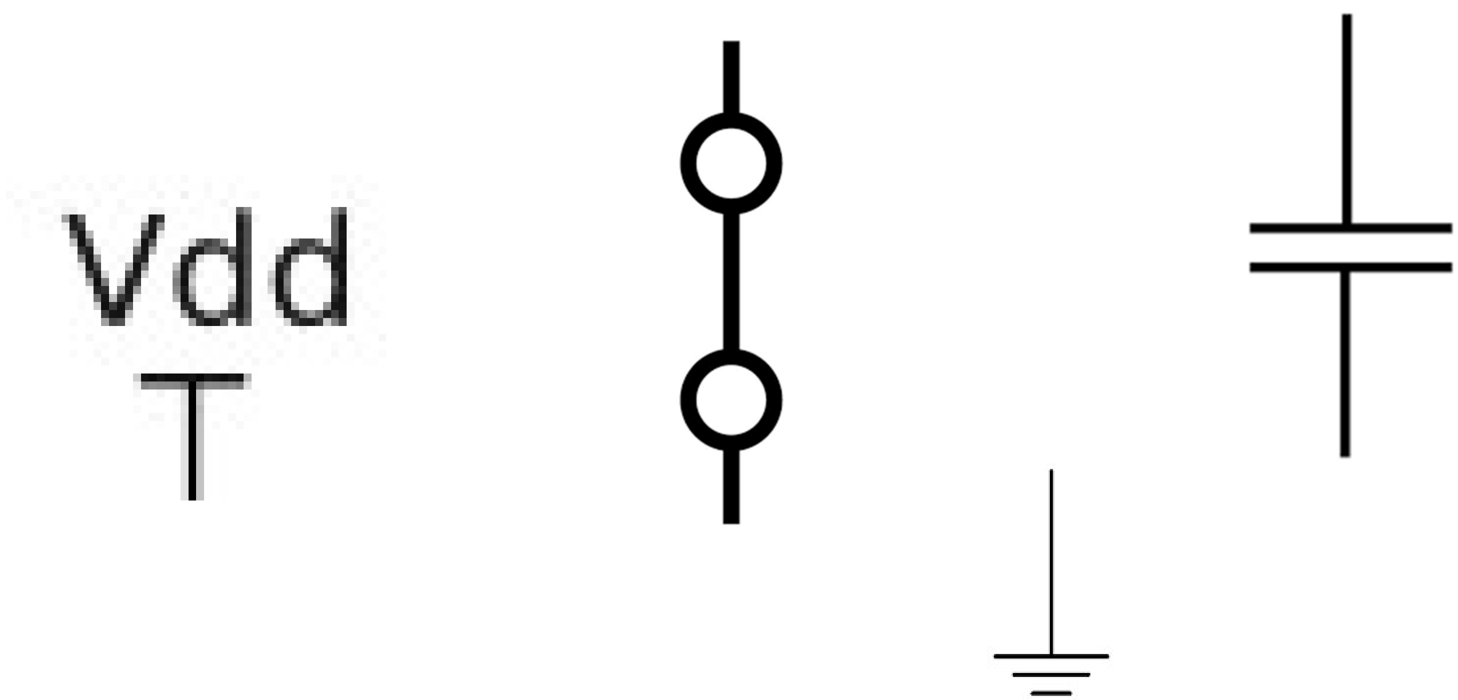
M4 – Off – open switch





=0.69*(r/2+r/2)*
(6c+15C) =


1
a
b
c
5


Vdd