MOHAMMED SATHAK A J COLLEGE OF ENGINEERING
Siruseri IT park, OMR, Chennai - 603103

LESSON PLAN

Department of Electronics and Communication Engineering

Name of the Subject	VLSI DESIGN	Name of the handling Faculty	Dr.I.Manju
Subject Code	EC8095	Year / Sem	III/VI
Acad Year	2021-2022	Batch	2019-2023

Course Objective

Study the fundamentals of CMOS circuits and its characteristics

Learn the design and realization of combinational & sequential digital circuits.

Architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology are discussed

Learn the different FPGA architectures and different testability of VLSI circuits

Course Outcome

Explain the concepts of digital building blocks using MOS transistor.

Design and construct combinational MOS circuits , Sequential Circuits.

Explain and analyse various delay, power strategies, Timing systems and testing

Design arithmetic building blocks and memory subsystems.

Apply and implement FPGA design flow

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB / PPT / NPTEL / MOOC / etc)	Blooms Level (L1-L6)	CO	PO
	UNIT I INTRODUCTION TO MOS TRANSISTOR						
1	MOS Transistor	T1,T2	1	BB,PPT	L1	CO1	PO1
2	Long-Channel I-V Charters tics	T1,T2	1	BB,PPT	L2	CO1	PO1-PO3
3	Non ideal I-V Effects	T1,T2	1	BB,PPT	L2	CO1	PO1
4	C-V Charters tics	T1,T2	1	BB,PPT	L2	CO1	PO1-PO3
5	CMOS logic	T1,T2	1	BB,PPT	L2	CO1	PO1-PO3
6	DC Transfer characteristics	T1,T2	1	BB,PPT	L2	CO1	PO1-PO3
7	Inverter, Pass Transistor, Transmission gate	T1,T2	1	BB,PPT	L2	CO1	PO1-PO3
8	Layout Design Rules,Gate Layouts, Stick Diagrams	T1,R4	1	BB,PPT	L3	CO1	PO1-PO3
9	RC Delay Model, Elmore Delay	T1,T2	1	BB,PPT	L3	CO3	PO1-PO3
10	Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate	T1,T2	2	BB,PPT	L4	CO3	PO1-PO3
12	Scaling.	T1,T2	1	BB,PPT	L2	CO1	PO1

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
In-class activity - Problems on delay in combinational circuits.

Evaluation method :
Assignments on Problems on delay in combinational circuits.

	UNIT II COMBINATIONAL MOS LOGIC CIRCUITS						
13	Circuit Families: Static CMOS	T1,T2	2	BB,PPT	L3	CO2	PO1-PO5
15	Ratioed Circuits, Cascode Voltage Switch Logic	T1,T2	1	BB,PPT	L3	CO2	PO1-PO5
16	Dynamic Circuits	T1,T2	1	BB,PPT	L3	CO2	PO1-PO5
17	Pass Transistor Logic, Transmission Gates	T1,T2	1	BB,PPT	L3	CO2	PO1-PO5
18	Domino, Dual Rail Domino, CPL, DCVSPG	T1,T2	1	BB,PPT	L3	CO2	PO1-PO5
19	DPL, Circuit Pitfalls	T1,T2	1	BB,PPT	L2	CO2	PO1-PO5
20	Power: Dynamic Power, Static Power	T1,T2	1	BB,PPT	L2	CO3	PO1-PO3
21	Low Power Architecture.	T1,T2	1	BB,PPT	L2	CO3	PO1-PO3

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
In-class activity - Problems based on design of combinational circuits.

Evaluation method
Assignment on Problems based on design of combinational circuits.

	UNIT III SEQUENTIAL CIRCUIT DESIGN						
22	Static latches and Registers	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
23	Dynamic latches and Registers	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
24	Pulse Registers, Sense Amplifier Based Register	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
25	Pipelining	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
26	Schmitt Trigger	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
27	Monostable Sequential Circuits	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
28	Astable Sequential Circuits.	T2,R2	1	BB,PPT	L2	CO2	PO1-PO5
29	Timing Issues : Timing Classification Of Digital System	T2,R2	1	BB,PPT	L2	CO3	PO1-PO5
30	Synchronous Design.	T2,R2	1	BB,PPT	L3	CO3	PO1-PO5

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
Static/dynamic latches and Registers design.

Evaluation method
Assignment on Static/dynamic latches and Registers

	UNIT IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM						
31	Arithmetic Building Blocks: Data Paths	T2,R2	1	BB,PPT	L2	CO4	PO1-PO5, PO11,PO12
32	Adders	T2,R2	2	BB,PPT	L3	CO4	PO1-PO5, PO11,PO12
34	Multipliers	T2,R2	2	BB,PPT	L3	CO4	PO1-PO5, PO11,PO12
36	Shifters, ALUs	T2,R2	1	BB,PPT	L2	CO4	PO1-PO5, PO11,PO12
37	power and speed tradeoffs	T2,R2	1	BB,PPT	L2	CO4	PO1-PO5, PO11,PO12
38	Case Study: Design as a tradeoff.	T2,R2	1	BB,PPT	L4	CO4	PO1-PO5, PO11,PO12
39	Memory Architectures and Building Blocks	T2,R2	1	BB,PPT	L2	CO4	PO1-PO5, PO11,PO12
40	Memory Core, Memory Peripheral Circuitry	T2,R2	1	BB,PPT	L3	CO4	PO1-PO5, PO11,PO12

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
Different types of Adders

Evaluation method
Tutorials Case studies on Adders

	UNIT V IMPLEMENTATION STRATEGIES AND TESTING						
41	FPGA Building Block Architectures	T1,R1	2	BB,PPT	L2	CO5	PO1-PO3, PO12
43	FPGA Interconnect Routing Procedures	T1,R1	1	BB,PPT	L2	CO5	PO1-PO3, PO12
44	Design for Testability: Ad Hoc Testing	T1,R1	1	BB,PPT	L2	CO3	PO1-PO3, PO12
45	BIST	T1,R1	2	BB,PPT	L2	CO3	PO1-PO3, PO12
47	IDDQ Testing, Design for Manufacturability	T1,R1	1	BB,PPT	L2	CO3	PO1-PO3, PO12
48	Boundary Scan.	T1,R1	2	BB,PPT	L2	CO3	PO1-PO3, PO12

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
Implementation of circuits using FPGA

Evaluation method: MCQ/ Quizzes on FPGA

Content Beyond the Syllabus Planned

1	Recap of Digital logic Circuits
2	Introduction to FINFET circuits

Text Books

1	Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective‖, 4th Edition, Pearson , 2017 (UNIT I,II,V)
2	Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective‖, Second Edition , Pearson , 2016.(UNIT III,IV)

Reference Books

1	M.J. Smith, —Application Specific Integrated Circuits‖, Addisson Wesley, 1997
2	Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition McGraw Hill Education,2013
3	Wayne Wolf, —Modern VLSI Design: System On Chip‖, Pearson Education, 2007
4	R.Jacob Baker, Harry W.LI., David E.Boyee, —CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.

Website / URL References

1	https://nptel.ac.in/courses/117/101/117101058/
2	https://nptel.ac.in/courses/108/107/108107129/
3	https://www.egr.msu.edu/classes/ece410/

Blooms Level

Level 1 (L1) : Remembering **Level 2 (L2) : Understanding** **Level 3 (L3) : Applying**	Lower Order Thinking	Fixed Hour Exams	Level 4 (L4) : Analysing Level 5 (L5) : Evaluating Level 6 (L6) : Creating		Higher Order Thinking	Projects / Mini Projects

Mapping syllabus with Bloom's Taxonomy LOT and HOT

Unit No	Unit Name	L1	L2	L3	L4	L5	L6	LOT	HOT	Total
Unit 1		1	7	2	2	0	0	10	2	12
Unit 2		0	3	6	1	0	0	9	1	10
Unit 3		0	8	1	0	0	0	9	0	9
Unit 4		0	4	5	1	0	0	9	1	10
Unit 5		0	9	0	0	0	0	9	0	9
Total		1	31	14	4	0	0	46	4	50
Total Percentage		2.00	62.00	28.00	8.00	0.00	0.00	92.00	8.00	100.00

CO PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2									1		
CO2	3	3	3	2	2						1	1	2	
CO3	3	3	3	2	2						1	1	2	
CO4	3	3	3	3	3						3	3	2	
CO5	3	2	2									3	2	
Avg	**3**	**2.6**	**2.6**	**1.4**	**1.4**						1	1.8	1.6	

Justification for CO-PO mapping

CO1	High correlation for PO1 and medium correlation for PO2,PO3 is given as the CO2 can be used to apply knowledge of engineering to Identify , formulate and provide solutions.
CO2	High correlation for PO1-PO3 is given as the CO2 can be used to apply knowledge of engineering to Identify , formulate and provide solutions amd medium correlation for PO4,PO5 provide solutions by using relevant techniques and tools. Medium correlation for PSO1 is given as filters are required for the design of analyze, design and develop solutions..
CO3	High correlation for PO1-PO3 is given as the CO3 can be used to apply knowledge of engineering to Identify , formulate and provide solutions and medium correlation for PO4,PO5 provide solutions by using relevant techniques and tools.Medium correlation for PSO1 is given as filters are required for the design of analyze, design and develop solutions..
CO4	High correlation for PO1-PO5 is given as the CO4 can be used to apply knowledge of engineering to Identify , formulate and provide solutions by using relevant techniques and tools.High Correlation for PO11,PO12 is given as the design of sub systems require project management and life long learning .Medium correlation for PSO1 is given as filters are required for the design of analyze, design and develop solutions..
CO5	High correlation for PO1,medium correlation for PO2,PO3 for CO5 can be used to apply knowledge of engineering to Identify , formulate and provide solutions.High Correlation for PO12 is given as the knowledge on new FPGA and testing techniques require life long learning.Medium correlation for PSO1 is given as filters are required for the design of analyze, design and develop solutions..

3	**High level**	**2**	Moderate level	**1**	Low level

Name & Sign of Faculty Incharge : Dr I.Manju

Name & Sign of Subject Expert :

Head of the Department : Mr Kamaraj

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