MOHAMMED SATHAK A J COLLEGE OF ENGINEERING

Siruseri IT park, OMR, Chennai - 603103

LESSON PLAN

Department of Electronics and Communication Engineering

Name of the Subject	COMPUTER ARCHITECTURE AND ORGANIZATION	Name of the	R.MUTHU PANDEESWARI
Subject Code	EC8552	Year / Sem	III/V
Acad Year	2022-2023	Batch	2020-2024

Course Objective

To make the students understand the basic structure and operation of digital computer

To familiarize with thw implementation of fixed point and floating point arithmetic operations

To study the design of data path unit and control unit for the processor

To understand the concepts of various memories and interfacing

To introduce the parallel processing techniques

Course Outcome

Upon completion of the course, the students will be able to:

CO1.Describe data representation, instruction formats and a operation of a digital computer

CO2.Illustrat the fixed point and floating point operation for ALU operation

CO3.Discuss about implementation schemes of control unit and pipeline performance

CO4.Explain the concept of various memories,interfacing and organization of multiple processor

CO5.Discuss paralell processing technique and unconventional architectures

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB / PPT / NPTEL	Blooms Level (L1-L6)	CO	PO
	UNIT I COMPUTER ORGANIZATION AND INSTRUCTION						
1	Basics of a computer Evolutions and Ideas	T1	1	PPT	L1	CO1	PO1
2	Technology,Performance	T1	1	BB	L2	CO1	PO1
3	Power wall	T1	1	BB	L2	CO1	PO1
4	Uniprocessors to multiprocessors	T1	1	BB	L1	CO1	PO1
5	Conditional Statements	T1	1	BB	L2	CO1	PO1
6	Addresing and addressing modes	T1	1	PPT	L2	CO1	PO1 &2
7	Instructions operations and Operands	T1	1	PPT	L2	CO1	PO1 &2
8	Representing instructions	T1	1	PPT	L2	CO1	PO1 &2
9	Logical Operations and Control Operations	T1	1	PPT	L2	CO1	PO1 &2
	Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Quiz						
	Evaluation method : Test						
	UNIT II C ARITHMETIC						
10	Fixed Point Addition	T1	1	BB	L2	CO2	PO1 &2
11	Fixed point Subtraction	T1	1	PPT	L2	CO2	PO1 &2
12	Fixed point Multiplicatio	T1	2	BB	L3	CO2	PO1 &2
13	Fixed Point Division	T1	2	BB	L3	CO2	PO1 &2
14	Floating point arithmetic	T1	1	BB	L3	CO2	PO1 &2
15	High performance arithmetic	T1	1	BB	L2	CO2	PO1 &2
16	Subword paralellism	T1	1	PPT	L2	CO2	PO1 &2
	Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Assignment						
	Evaluation method : Mark based						
	UNIT III - THE PROCESSOR						
17	Introduction, Logic design conventions	T	1	BB	L2	3	PO1 &3
18	Building a Datapath	T	1	BB	L2	3	PO1 &3
19	A simple Implementation scheme	T	1	BB	L2	3	PO1 &3
20	An overview of Pipelining	T	1	BB	L1, L2	3	PO1 &3
21	Pipelined Datapath and Control	T	1	BB	L2	3	PO1 &3
22	Data Hazards	T	1	BB	L4	3	PO1 &3
23	Forwarding versus stalling	T	1	PPT	L1, L2	3	PO1 &3
24	Contro Hazards	T	1	PPT	L1	3	PO1 &4
25	Exceptions	T	1	PPT	L2	3	PO1 &5
26	Paralellism via instructions	T		PPT	L3	3	PO1 &6
	Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Assignment						
	Evaluation method : Mark based						
	UNIT IV MEMORY AND I/O ORGANIZATIONS						
27	Memory hierarchy	T1	1	BB	L2	CO3	PO1 &3
28	Memor chip organization	T1	1	PPT	L2	CO3	PO1 &3
29	Cache memory	T1	1	BB	L2	CO3	PO1 &3
30	Virtual memory	T1,W1	1	PPT	L2	CO3	PO1 &3
31	Paralell bus architectures	T1,W1	1	BB	L2	CO3	PO1 &3
32	Internal Communication methodlogies	T1,W1	1	PPT	L2	CO3	PO1 &3
33	Serial bus architectures	T1,W1	1	PPT	L2	CO3	PO1 &3
34	Mass storage	T1	1	PPT	L2	CO3	PO1 &3
35	Input Output devices	T1	1	BB	L2	4	PO1 &3
	Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Role Play						
	Evaluation method : Marks based on their presentation and points						
	UNIT V ADVANCED COMPUTER ARCHITECTURE						
36	Paralell processing archirectures and challenges	T1	1	PPT	L2	CO4	PO1
37	Hardware multithreading	T1	2	PPT	L2	CO4	PO1
38	Multicore and shared memory multiprocessors	T1	1	PPT	L2	CO4	PO1
39	Introduction to GPU	T1	1	PPT	L2	CO4	PO1
40	Clusters and warehouse scale computers	T1	2	PPT	L2	CO4	PO1
41	Network topologies	T1	2	PPT	L2	CO4	PO1
	Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any: Assignment						
	Evaluation method : Marks based						

1	1.Hardwired programmed control
2	2.Micro programmed control

Text Books

1	**David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan auffman / lsevier, Fifth edition, 2014.**
2	**Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian, Computer Organization and Embedded Systems, Sixth Edition, Tata McGraw Hill, 2012.**

Reference Books

1	**William Stallings "Computer Organization and Architecture", Seventh Edition, Pearson Education, 2006.**
2	**Vincent P. Heuring, Harry F. Jordan, "Computer System Architecture", Second Edition, Pearson Education, 2005.**
4	**Govindarajalu, "Computer Architecture and Organization, Design Principles and Applications", first edition, Tata McGraw Hill, New**

Website / URL References

1	http://nptel.ac.in/
3	https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials

Blooms Level

Level 1 (L1) : Remembering	Lower	Fixed	**Level 4 (L4) : Analysing**		Higher	Projects /
Level 2 (L2) : Understanding	Order	Hour	**Level 5 (L5) : Evaluating**		Order	Mini
Level 3 (L3) : Applying	Thinking	Exams	**Level 6 (L6) : Creating**		Thinking	Projects

Mapping syllabus with Bloom's Taxonomy LOT and HOT

Unit No	Unit Name	L1	L2	L3	L4	L5	L6	LOT	HOT	Total
Unit 1	COMPUTER ORGANIZATIONS AND	2	7	0	0	0	0	9	0	9
Unit 2	ARITHMETIC	0	4	**5**	**0**	**0**	**0**	9	0	9
Unit 3	THE PROCESSOR	0	9	**0**	**0**	**0**	**0**	9	0	9
Unit 4	MEMORY AND I/O ORGANIZATION	0	9	**0**	**0**	**0**	**0**	9	0	9
Unit 5	ADVANCED COMPUTER	0	7	**1**	**1**	**0**	**0**	8	1	9
Total		2	36	6	1	0	0	44	1	45
Total Percentage		4.44	80.00	13.33	2.22	0.00	0.00	97.78	2.22	100

CO PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	3	2
CO2	3	2	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	3	2
CO3	3	2	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	3	2
CO4	3	2	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	3	2
CO5	3	2	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	3	2
Avg	**3**	**2**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	3	2

Justification for CO-PO mapping

CO1	Describe data representation, instruction formats and a operation of a digital computer
CO2	Illustrat the fixed point and floating point operation for ALU operation
CO3	Discuss about implementation schemes of control unit and pipeline performance
CO4	Explain the concept of various memories,interfacing and organization of multiple processor
CO5	Discuss paralell processing technique and unconventional architectures

3	**High level**	**2**	**Moderate level**	**1**	Low level

Name & Sign of Faculty Incharge : R.MUTHU PANDEESWARI

Name & Sign of Subject Expert :

Head of the Department :

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