Unit - I

Power Semiconductor Devices

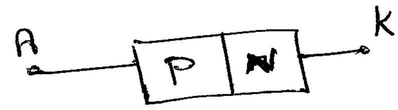
Study of Switching Devices:-

I DIODE:-

VI Characteristics of Diode:-

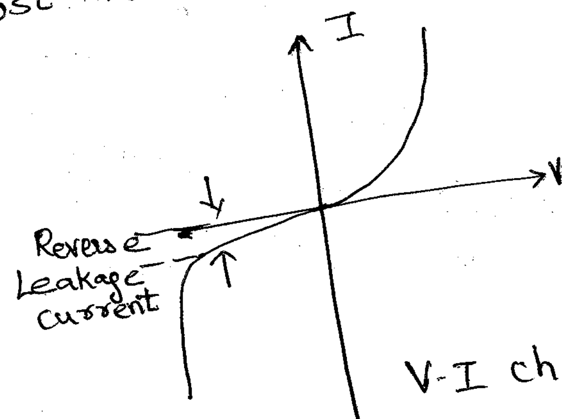
* Power diode is a two terminal pn junction device
* pn junction is normally formed by Alloying, diffusing and epitaxial growth
* Two terminals are anode (A) and Cathode (K).

Diode symbol



Sectional view

* When anode potential is +Ve with respect to cathode, diode is forward biased and it will conducts
* When Cathode potential is +Ve with respect to anode, diode is reverse biased.
* In Reverse biased Condition ~~and~~ a small ~~revers~~ reverse current flows known as leakage current.
* This leakage current increases slowly in magnitude with reverse voltage untill breakdown or avalanche voltage is reached.
* At Break down voltage diode is turned off in reverse direction.
* In most Practical case diode acts as a switch



V-I characteristics of Diode

The diode current equation (schottky diode) is given by

$$I_D = I_s\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

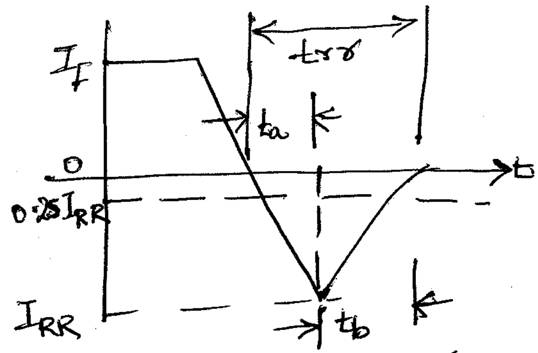
- I_D - Current through diode A
- I_s - leakage current or reverse saturation current mA or μA
- η - empirical constant known as emission coefficient or ideality factor whose value varies from 1 to 2
- V_T - Thermal voltage V
- V_D - Diode voltage V

$$V_T = \frac{KT}{q}$$

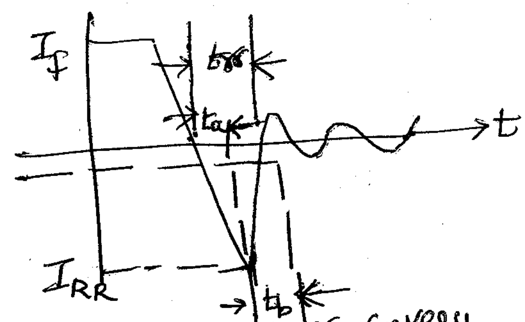
- K - Boltzmann's constant
- T - Absolute temperature
- q - electron charge

<u>Reverse Recovery characteristics</u>:-

* The current in a forward biased junction diode is due to the net effect of majority and minority carriers.
* Once the diode is in forward biased, the forward current reduces to zero.
* When forward current reduces, the diode continues to conduct in the reverse direction due to the minority carriers which are stored in the pn junction.
* The diode continues to conduct due to minority ~~that remain st~~ carriers.
* The minority carriers require a certain time to recombine with opposite charges and to be neutralized. This time is known as <u>reverse recovery time</u> of the diode denoted by (t_{rr})
* The reverse recovery characteristics of the diode is shown.



Soft recovery



Abrupt recovery

Soft recovery type is more common.

<u>Reverse recovery time</u>:-

* Define as t_{rr} measured from initial zero crossing of the diode current to 25% of maximum or peak reverse current I_{RR}. The t_{rr} consist of two components t_a and t_b.

* t_a is due to the charge stored in the depletion region of the junction. representing the time between zero crossing and peak reverse current I_{RR}.

* t_b is due to charge storage in bulk semiconductor material.

* The ratio t_b/t_a is known as softness factor (SF).

$$t_{rr} = t_a + t_b.$$

Peak reverse current $I_{RR} = t_a \frac{di}{dt}$ —(1)

<u>Reverse recovery charge</u>:- The amount of charge carriers that flows across the diode in reverse direction ~~due to~~ from forward conduction to reverse blocking conduction.

$$Q_{RR} \cong \frac{1}{2} I_{RR} t_a + \frac{1}{2} I_{RR} t_b$$

$$= \frac{1}{2} I_{RR} (t_a + t_b) = \frac{1}{2} I_{RR} t_{rr}$$

$$I_{RR} = \frac{2 Q_{RR}}{t_{rr}} \quad \text{—(2)}$$

Substitute I_{RR} in eq ①

$$\frac{2Q_{RR}}{t_{rr}} = t_a \frac{di}{dt}$$

$$t_{rr} t_a = \frac{2Q_{RR}}{di/dt}$$

If t_b is negligible compared to t_a, and $t_a \approxeq t_{rr}$.

$$t_{rr}^2 = \frac{2Q_{RR}}{di/dt}$$

$$t_{rr} = \sqrt{\frac{2Q_{RR}}{di/dt}}$$

Sub t_{rr} in eq ②

$$I_{RR} = \sqrt{2Q_{RR}\frac{di}{dt}}$$

Reverse recovery time and peak reverse recovery current I_{RR} depend on the storage charge Q_{RR} and ~~reverse~~ rate of change of current di/dt.

Types of power Diodes:-

1. General purpose Diodes 2. Fast recovery diode
3. Schottky diodes.

1. General Purpose Diodes:-
   * It has high reverse recovery time, typically 25μs, used in low speed applications.
   * Current ratings vary from 1 A to several thousand of amperes and voltage varies from 50V to 5KV.

2. Fast Recovery Diodes:-
   * It has low recovery time, normally less than 5μs.
   * Most usely in dc-dc and dc-ac converter circuits.

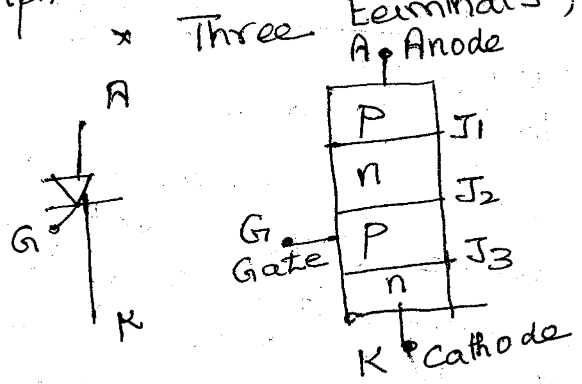
* Current ratings from less than 1A to hundred of amperes
* Voltage vary from 50V to 3KV.
* For voltages below 400V, epitaxial diodes provide faster switching speeds than diffused diode.
* for voltages above 400V, diffused diodes are prefered for faster switching speed.

3. <u>Schottky Diode</u>:

* Barrier potential exists between metal and a semiconductor to eliminate the charge storage problem in schottky Diode
* A layer of metal is deposited on a thin epitaxial layer of n type silicon.
* This potential barrier simulates the behaviour of p-n junction.
* forward voltage drop of ~~schottky~~ schottky diode is low. and leakage current is very high.
* Reverse voltage ratings are limited to 100V, and forward current ratings vary from 1A to 300 A.
* Used in High frequency instrumentation and switching power supplies.

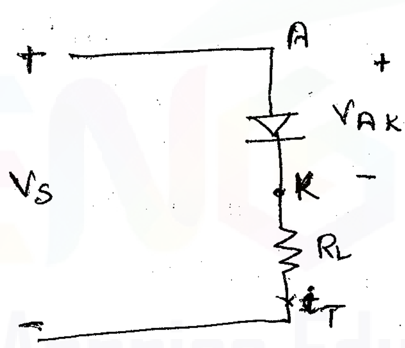
II <u>Thyristors (SCR)</u>

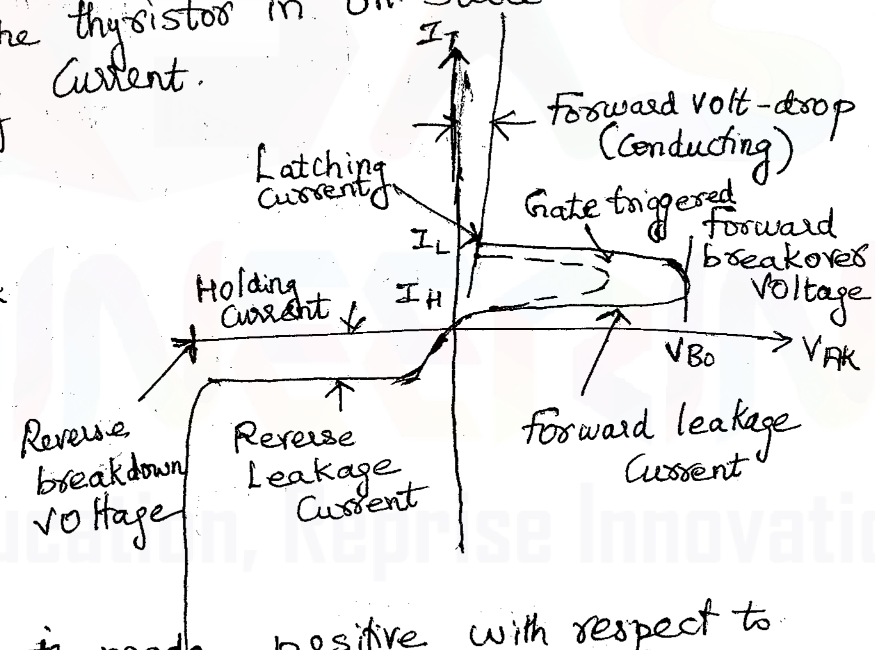
* It is a four layer semiconductor device of pnpn structure with three pn junctions.
* Three terminals, anode, cathode and gate.



* When anode is made +ve with respect to cathode, J_1 and J_3 junctions are forward biased (FB)

* J_2 is reverse biased (RB) and only a small leakage Current flows from anode to cathode.
* The thyristor is in forward blocking or off state and leakage current is known as off-state current I_D.
* When V_{AK} ↑, the R.B junction J_2 breaks which is known as avalanche breakdown and the voltage is called forward breakover voltage. voltage is called V_{BO}.
* Latching current is the minimum anode current required to maintain the thyristor in on state immediately after a thyristor has been turned on and the gate signal has been removed.
* Holding current is the minimum anode current to maintain the thyristor in on-state which is less than Latching current.

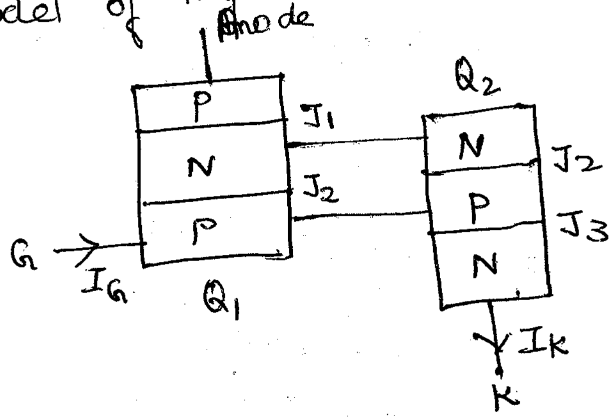


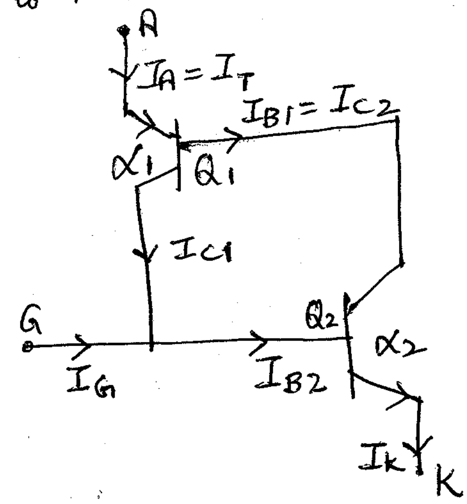


* When cathode is made positive with respect to anode, J_2 is F.B and J_1 & J_3 are R.B.
* The thyristor is in reverse blocking state and a reverse leakage current known as reverse current I_R flows through the device.
* When SCR is in forward blocking mode a gate pulse or anode cathode voltage is increased beyond breakover voltage to make the SCR to turn on. Which is called forward conduction mode. where the device acts like a closed switch.

Two transistor Model of Thyristor :-

Two complementary transistors, one pnp and other npn transistors Connected to form two transistor model of thyristor.





The collector current of a thyristor is related to emitter current I_E and the leakage current of Collector - base junction

$$I_C = \alpha I_E + I_{CBO}$$

Common base current gain $\alpha \simeq I_C / I_E$.

For transistor Q_1 $\quad I_{C1} = \alpha_1 I_A + I_{CBO1}$

I_{CBO1} is the leakage current for Q_1.

For transistor Q_2 $\quad I_{C2} = \alpha_2 I_K + I_{CBO2}$

$$I_A = I_{C1} + I_{C2} = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2}$$

Substitute $I_K = I_A + I_G$

$$I_A = \alpha_1 I_A + I_{CBO1} + \alpha_2 (I_A + I_G) + I_{CBO2}$$

$$I_A - \alpha_1 I_A - \alpha_2 I_A = I_{CBO1} + \alpha_2 I_G + I_{CBO2}$$

$$I_A \left(1 - (\alpha_1 + \alpha_2)\right) = I_{CBO1} + \alpha_2 I_G + I_{CBO2}$$

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

* The current gain α_1 and α_2 Varies with I_A and I_K.
* If ~~α_1~~ $(\alpha_1 + \alpha_2)$ approaches unity, denominator approaches zero, resulting in large anode current. and thyristor turns on with a small gate current.

Thyristor turn on methods :-

(a) Forward Voltage triggering:

* When V_{AK} (anode Cathode voltage) is increased with gate circuit open, the reverse biased junction J_2 will have an avalanche breakdown at a voltage called forward breakover voltage V_{BO}.

* The thyristor changes from off state to ON state characterised by a low voltage across it with large forward current.

* Forward voltage drop during ON state is of the order of 1 to 1.5V.

(b) Thermal Triggering (Temperature triggering).

* When the voltage applied between the anode and cathode is very near to its breakdown voltage, the device can be triggered by increasing its junction temperature.

* By increasing the temperature, R.B junction collapses making the device conduct. This method of triggering is known as the thermal triggering process.

(c) Radiation triggering (Light Triggering).

* With the held of external energy, electron hole pairs are generated in the device, thus increasing the number of charge carriers.

* This leads to instantaneous flow of current within the device and the triggering of the device.

* Light activated silicon controlled rectifier (LASCR) and light activated silicon controlled switch (LASCS) are examples of this type of triggering.

(d) <u>dv/dt triggering:-</u>

* J_1 and J_3 are forward biased, and junction J_2 becomes reverse biased.
* Reverse biased junction J_2 has the characteristics of capacitor due to charges existing across the junction.
* When forward voltage is suddenly applied, charging current will flow tending to turn the device ON.

$$i_c = \frac{dQ}{dt} = \frac{d}{dt}(C_j V) = C_j \frac{dV}{dt} + V \frac{dC_j}{dt}$$

rate of junction capacitance is negligible as compared to junction capacitance.

$$i_c = C_j \frac{dV}{dt}.$$

The rate of change of voltage across the device is large, the device may turn on even though the voltage appearing across the device is small.

(e) Gate Triggering:-

* Most commonly used method, by applying a positive signal at the gate terminal of the device, which will triggered before the specified breakover voltage
* Conduction of SCR can be controlled by varying the gate signal within the specified values of maximum and minium gate currents.
* Signal is applied between gate and cathode of the device. It is of three types. They are dc signals, pulse signals or ac signals.

a) DC gate triggering:-

* A proper magnitude dc voltage is applied between the gate and cathode of the device with gate positive with respect to cathode.

Drawbacks:-

* Both power and control circuits are not isolated from dc.
* Continuous gate signals produces more losses.

b) AC gate triggering:

* AC source is used for gate signal. This scheme provides the proper isolation between the power and the control circuits.
* Gate drive is maintained during positive half cycle where the device is turned ON
* During negative half cycle reverse voltage is applied where the device is turned off.

Drawback:

1. Seperate transformer is required to step down the ac supply.

c) Pulse gate triggering:-

* The pulse appears periodically or sequence of high frequency pulses. This is known as Carrier frequency gating.

Advantage:

* No need of applying continuous signals and hence gate losses are very much reduced.
* Electrical isolation is provided between the main device supply and its gating signals.

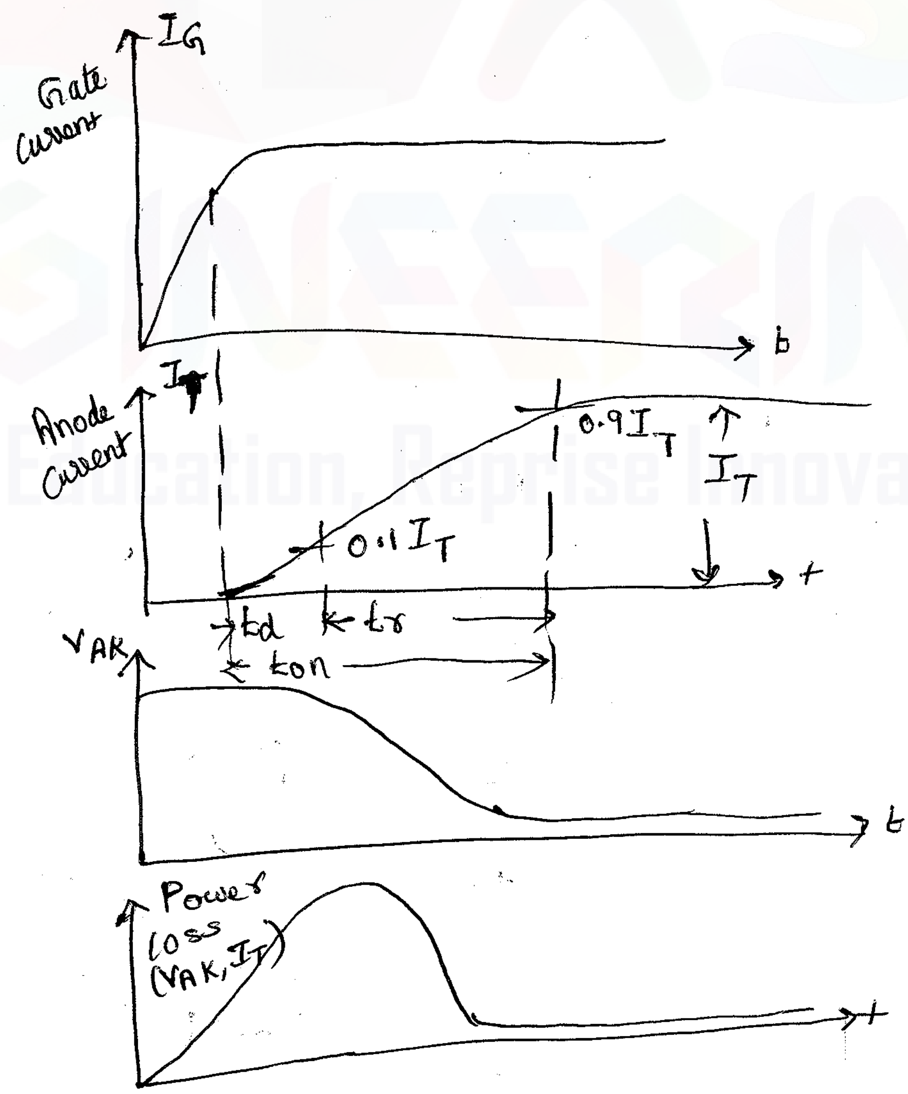
Dynamic turn on switching characteristics

* The transition from one conduction state to non conduction state does not take place instantaneously, and it occupies a finite period of time.

* The total turn on time t_{on} of the SCR is subdivided into two distinct periods, called delay time and rise time.

Delay time t_d:-

* The time between the instant at which gate current reaches 90% of final value and the anode current reaches 10% of final value.



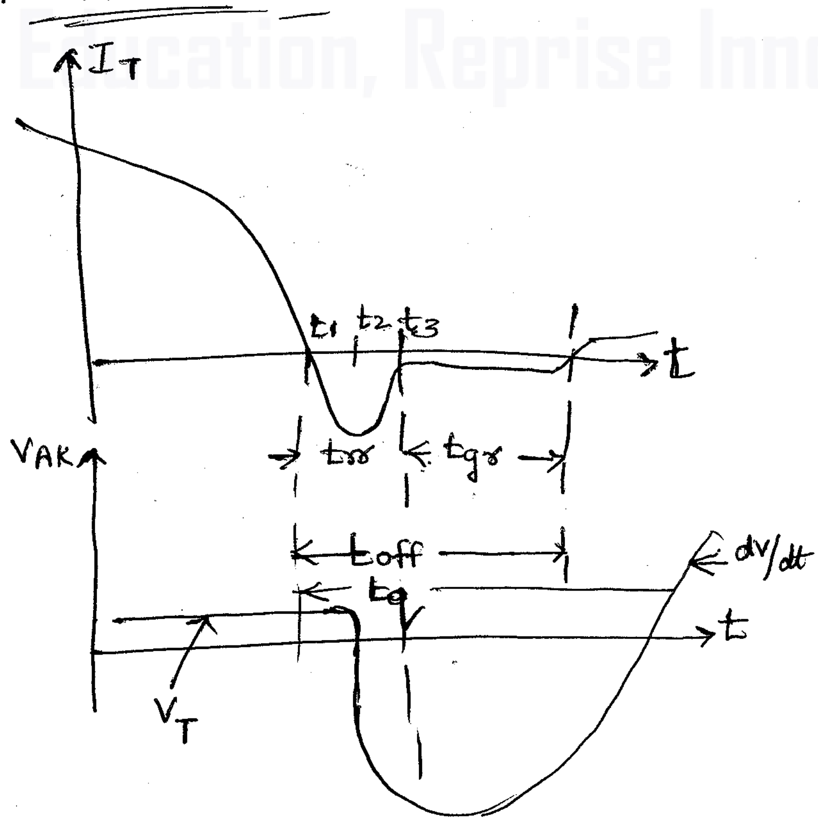
Rise time t_r

The time required for anode current to rise from 10 to 90% of its final value.

Turn on time t_{on}:

* It is the sum of delay and rise time, which of 1 to 4 μs.
* Width of firing pulse should be more than 10 μs.
* Amplitude of gate pulse should be 3 to 5 times the minimum gate current required to trigger the SCR.
* During rise time SCR carries large current and appreciable forward voltage.
* To limit the current a small inductor is inserted in anode circuit.
* The power curve shows the switching losses of the device, which may be significant in high frequency applications.

Turn off Mechanism:



* The SCR can be turned off by reducing the forward current to a level below that of the holding current.
* Process of turn off is called Commutation.
* After reducing the anode current to zero, if a forward voltage is applied immediately it will not block the forward voltage the device starts to conduct again, unless the device is reverse biased for a finite period before a forward anode voltage can be reapplied.

Turn off time:

The minimum interval at which the anode current becomes zero and the instant at which the device is capable of blocking the forward voltage. The turn off time is divided into ~~three~~ two intervals, reverse recovery time and gate recovery time.

* At t_1, anode forward current becomes zero
* During the reverse recovery time t_{rr}, anode current flows in the reverse direction.
* At t_2, a reverse anode voltage is developed, and reverse recovery current continues to decrease.
* At t_3, J_1 and J_3 block reverse voltage, but forward voltage cannot be blocked due to carriers called trapped charges at the junction J_2.
* At the interval t_3 to t_4 these carriers recombine.
* At t_4 the recombination is complete and forward voltage can be applied at this instant. SCR turn off time is the interval between t_4 and t_1.

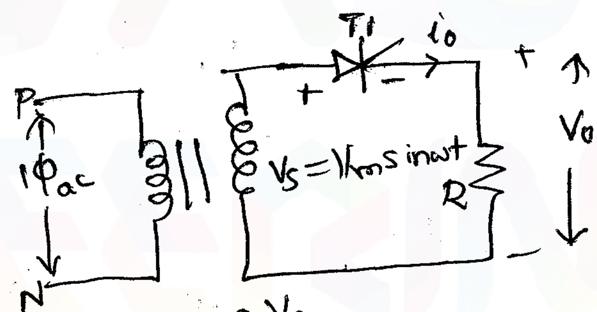
Commutation of SCR

The process of ~~burning~~ turning off a thyristor is called Commutation. Many techniques to Commutate a thyristor. These can be classified as

1. Line Commutation (or) Natural Commutation
2. forced commutation.

Natural Commutation:

The thyristor is automatically turned off during the negative half cycle of input voltage if the source voltage is ac. This Commutation is known as Natural or line Commutation. This method of Commutation is applied to phase Controlled rectifiers, ac voltage Controller, line commutated inverters and step down cyclo converters.



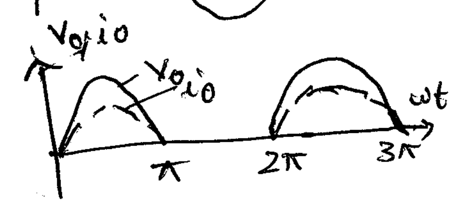
When T_1 is fired at $\omega t = 0$ during positive half cycle

$V_0 = V_s$.

At $\omega t = \pi$, $V_s = 0$, $V_0 = 0$,

$i_0 = 0$

When T_1 is turned off. during negative half cycle.



Forced Commutation:-

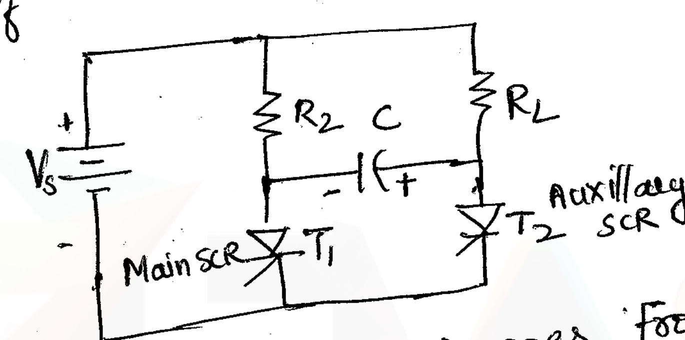
In case of dc circuits for switching off the thyristors the forward current of the thyristor is forced to zero by an additional Circuitry called Commutation Circuit. The Commutation is called forced Commutation.

Capacitor Commutation:-

In DC circuits, the SCR can be turned off by switching the anode current to an alternate path for sufficient time to allow the SCR to receive its blocking capability.

* When SCR is on, transistor is in off state.

To turn off SCR, a positive pulse is applied to base of ~~transistor Q turning it on.~~

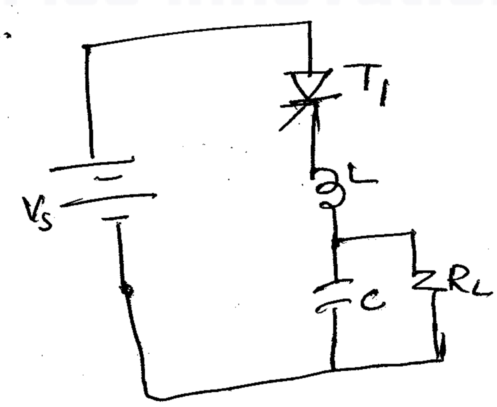


* When T_1 conducts, capacitors charges from the source voltage through R_L.
* To turn off T_1 auxillary thyristor T_2 is turned on.
* ~~by~~ Reverse voltage is applied to the thyristor T_1 to turn off.

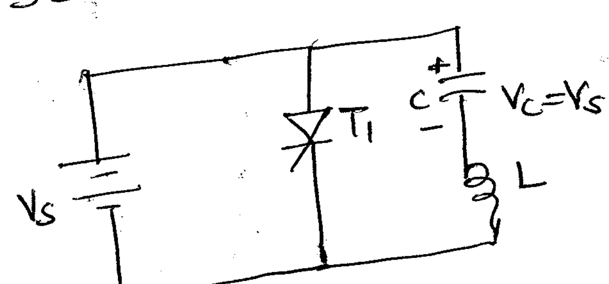
Commutation by Resonance:-

* LC circuit forms a resonance.

The ~~undamp~~ Underdamped LC resonating circuit in series with the load applies a reverse voltage to SCR to turn off.



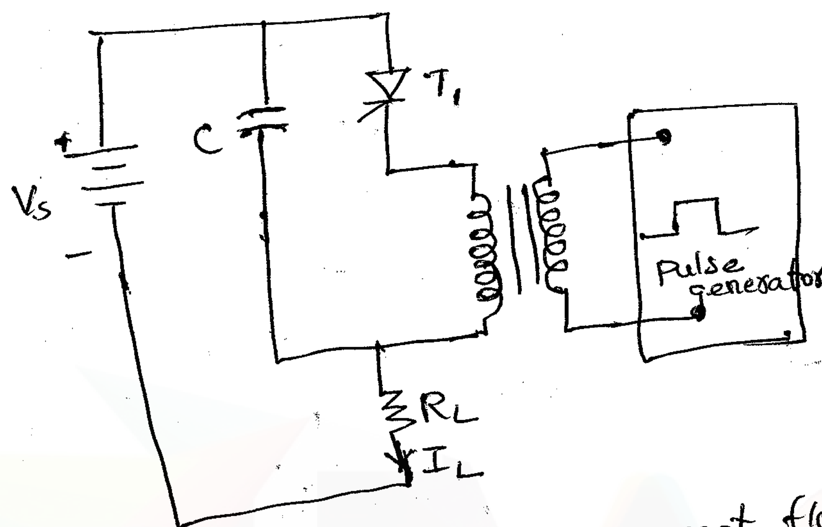
Series resonance.



Parallel Resonance

Commutation by external source:

* The external Source is in the form of pulse.
* The pulse generator reverse biases the SCR T_1 and thus turns it off.
*



* When SCR T_1 is triggered the current flows through T_1 and secondary of pulse transformer and load.
* To turn off SCR T_1, a positive pulse from the pulse transformer is applied to the cathode of SCR T_1.
* The Capacitor is charged for only 1V. and can be assumed short circuit during the period of commutation.

Snubber Circuit of SCR:-

* To protect the thyristor from large (di/dt) during turn on and large dv/dt during turn off. a snubber circuit is essential

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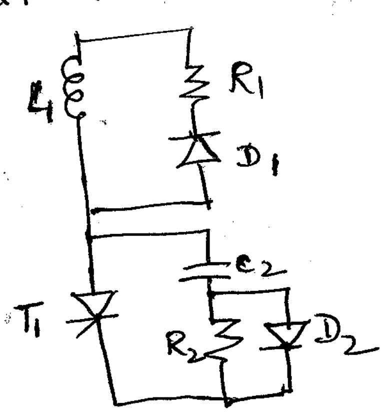
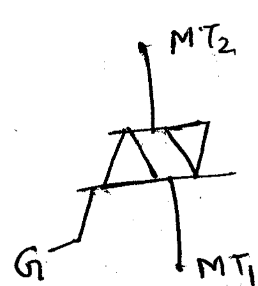
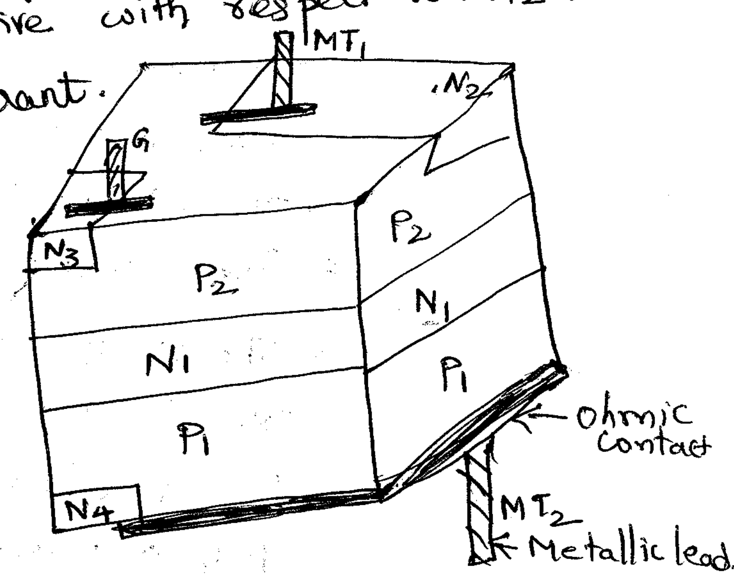


* Inductor L_1 protects T_1 from large di/dt during turn on process
* The circuits by R_1 and D_1 allows the discharging of L_1 when the thyristor is turned off.
* The snubber circuit is made by R_2 C_2
* The auxillary circuit made by D_2 and R_2 allows the discharging of C_2 when the thyristor is turned on.
* The circuit of C_2 and L_1 limits the value of dv/dt across the thyristor during forward blocking.

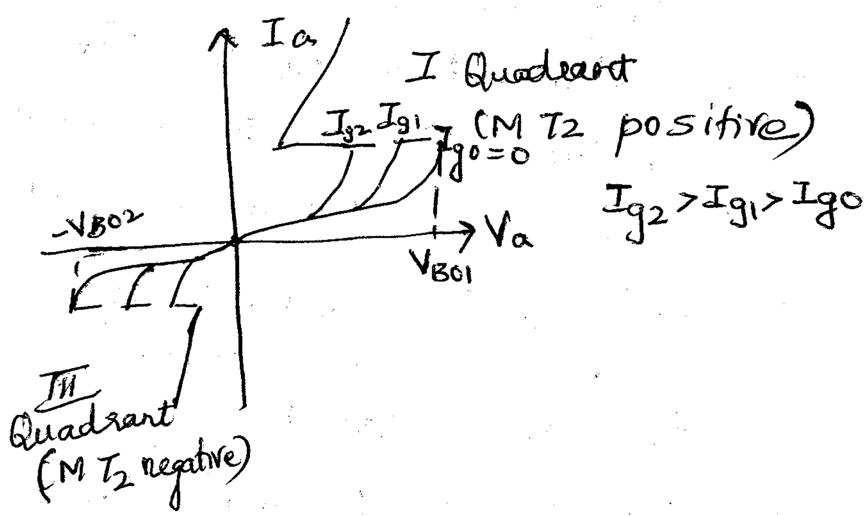
III BIDIRECTIONAL TRIODE THYRISTOR (TRIAC)

* Two thyristors connected in antiparallel which are integrated in single structure is called as TRIAC (Triode ac switch)
* Three terminals MT_1, MT_2 and gate G.
* TRIAC can conduct in both direction
* MT_2 is positive with respect to MT_1 for first quadrant
* MT_1 positive with respect to MT_2 for third quadrant.





TRIAC Characteristics



Triggering Modes of Triac:

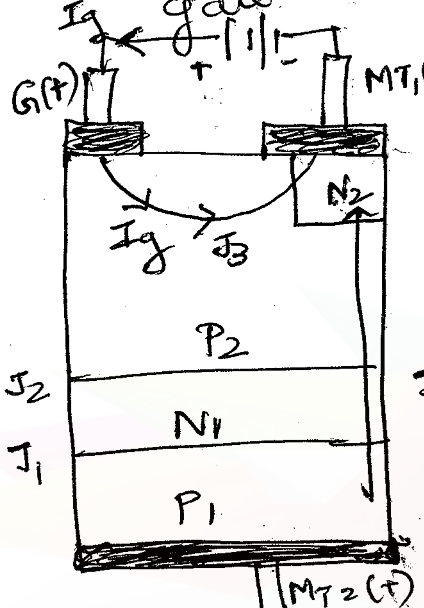
1. MT_2 positive, positive gate current (Mode 1)

* Gate current is positive with respect to MT_1. Gate current flows from gate lead to the terminal MT_1 through P_2N_2 junction like an SCR
* ~~When gate~~ sufficient charge is injected into P_2 layer, reverse biased junction N_1P_2 breaks down.
* Triac starts conducting through $P_1N_1P_2N_2$ layers.
* Triac operates in 1st quadrant.

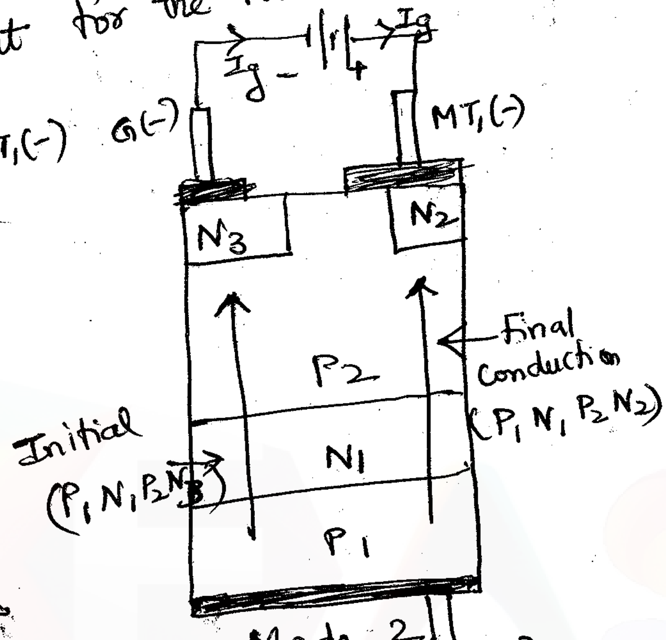
2. MT_2 positive, gate current negative (Mode 2)

* Gate current flows through P_2N_3 junction and reverse biased junction N_1P_2 is forward biased as a normal thyristor
* Triac conducts through $P_1N_1P_2N_3$ layers.
* The voltage drop falls but P_2N_3 rises towards the anode potential of MT_2.
* P_2 is clamped to the cathode potential of MT_1 a potential gradient exists across layer P_2, the left hand being higher than right hand region.

* Current is established in layer P_2 from left to right which forward biased P_2N_2 junction.
* Finally $P_1N_1P_2N_2$ begins to conduct as auxillary structure.
* This is called as Pilot SCR. which is an auxillary structure
* The anode current of pilot SCR serves as the gate current for the main SCR.



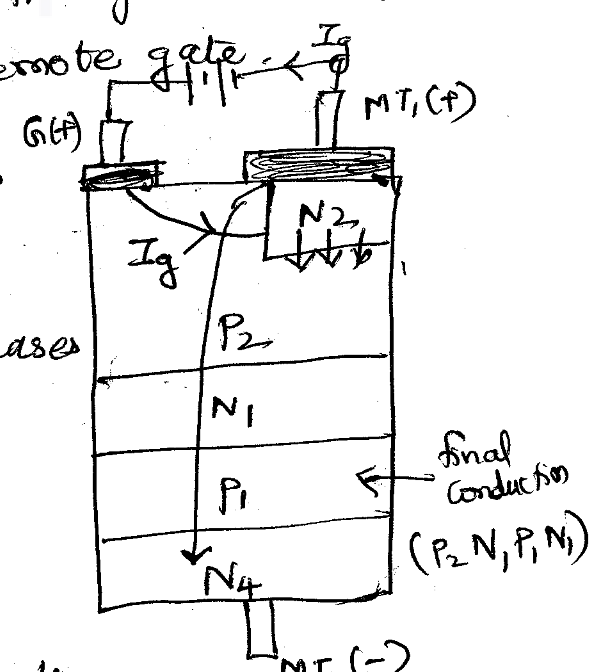
Mode 1



Mode 2

3. Mode 3: MT_2 negative positive gate current.

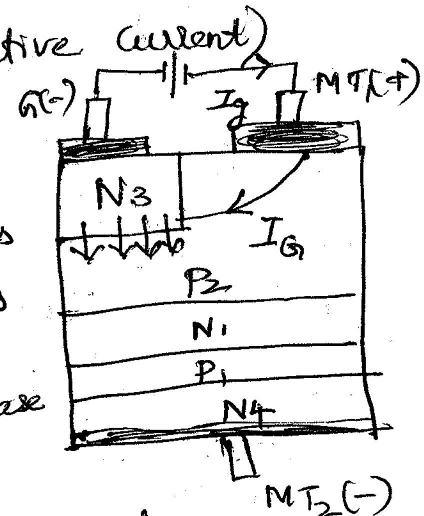
* The device operates in third quadrant during conduction.
* The turn on is by gate control
* The triac conducts through $P_2N_1P_1N_4$ with N_2 actings a remote gate.



* The gate current forward biases P_2N_2 junction
* N_2 injects electrons into P_2N_1 junctions which increases the current.
* The holes injected from P_2 diffuse through N_1 and arrive at P_1.
* More electrons from N_4 diffuse into P_1 to neutralize the positive space charge.

* The triac is turned on by remote gate N_2, where the device is less sensitive in third quadrant with positive gate current

4. Mode 4 (MT_2 negative, negative current)



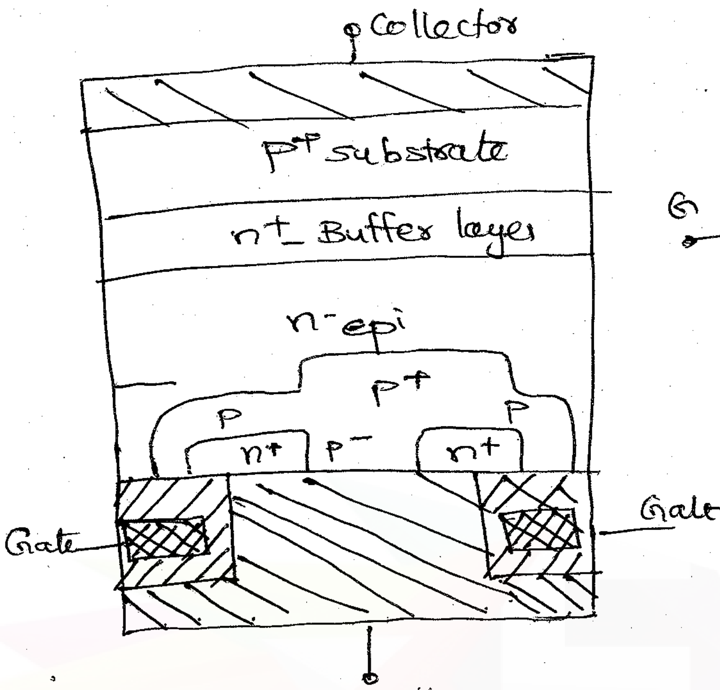
* N_3 acts as remote gate
* Gate current forward biases P_2N_3 junction and electrons are injected into P_2N_1 junction causing an increase of current P_1N_1.
* $P_2N_1P_1N_4$ turns on by regenerative action. ~~breaking~~.
* Sensitive is more in 1^{st} quadrant when +ve gate current. and also in III^{rd} quadrant with negative gate current.
* Sensitive in less in 1^{st} quadrant when -ve gate current.
* III^{ly} in third quadrant with positive gate current.

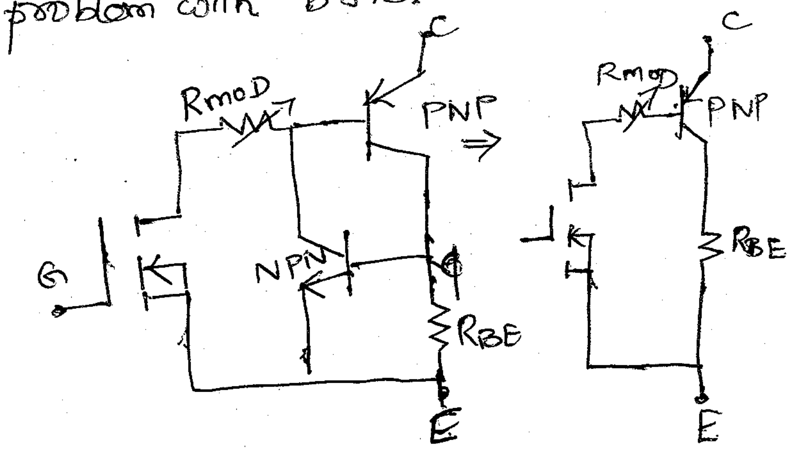
Advantages of Triac:
* Triac can be triggered with positive or negative polarity
* Neet a single heat sink of larger size, whereas antiparallel SCR needs two heat sinks of smaller size
* Needs single fuse for protection
* SCR is connected in parallel to a diode to protect against reverse voltage

Disadvantage:
1. Low dv/dt rating
2. Trigger circuit needs a careful consideration since triac conducts in both direction
3. Triacs are available small in rating.

INSULATED GATE BIPOLAR TRANSISTORS (IGBTS)

It has high input impedance of the MOSFET and low on state conduction losses like BJTs. There is no second breakdown problem with BJTs.





p+ Substrate is responsible for minority carrier injection into n-region. An IGBT is made of four alternate PNPN Layers. The n+ buffer layer and wide epi base reduce the gain of NPN terminal, thereby avoiding Latching.

IGBT have two structures:

1. Punch through (PT)
2. Non punch through (NPT).

In PT structure, switching time is reduced by use of heavily doped n-buffer layer in the drift region near the collector. In the NPT structure, carrier life time is kept more than that of a PT structure, which causes conductivity modulation of the drift region and reduces the on-state voltage drop.

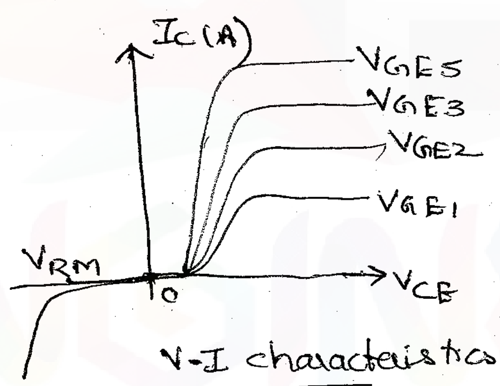
An IGBT is voltage controlled device, similar to power MOSFET. When the gate is made positive with respect to emitter for turn-on, ~~by~~ n-carriers are drawn into the p-channel near the gate region, this results in a forward bias of the base of the npn transistor, which thereby turns on. An IGBT is turned on by just applying a positive gate voltage to open the channel for n-carriers and is turned off ~~by just applying a positive gate voltage to open the channel for n-carriers~~

and is ~~the~~ turned off by removing the gate voltage to close the channel. It requires a very simple driver circuit. It has lower switching and conducting losses. The terminals of IGBT as gate, drain and source.

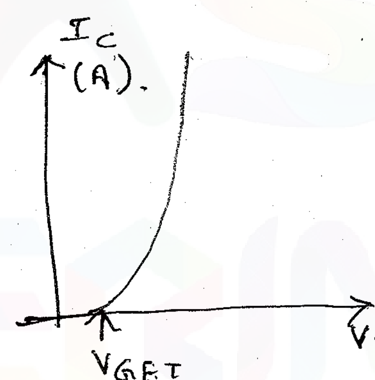
~~Switching~~ static V-I characteristics of IGBT:-

The plot of collector current I_C versus collector-emitter voltage V_{CE} for various values of gate-emitter voltages. The controlling parameter is gate emitter voltage because IGBT is a voltage controlled device. The transfer characteristics is a plot of collector current I_C versus gate-emitter voltage V_{GE}. When V_{GE} is less than the threshold voltage V_{GET} IGBT is in the off state.

When the device is off, junction J_2 blocks forward voltage and in case reverse voltage appears across collector and emitter, junction J_1 blocks it.



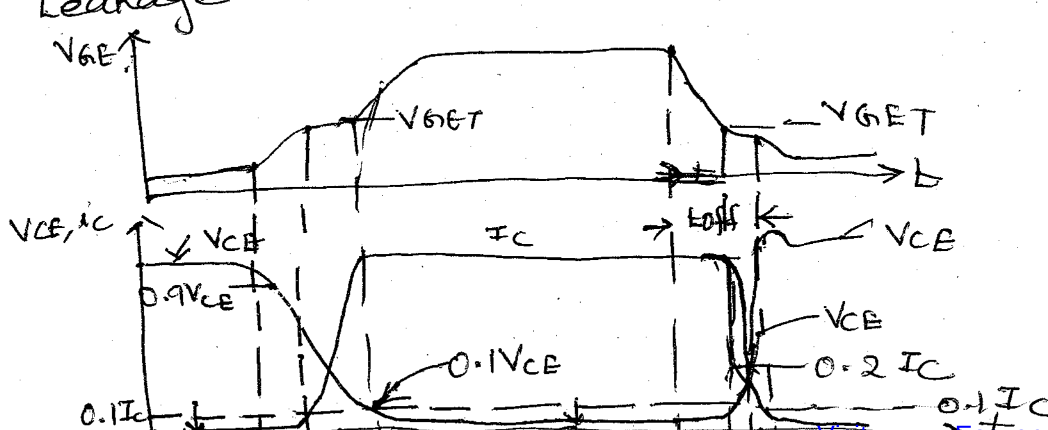
V-I characteristics



Transfer characteristics

Switching characteristics:

The turn-on time is defined as the time between the instants of forward blocking to forward on state. Turn on time is composed of delay time t_{dn} and rise time t_r. (ie) $t_{on} = t_{dn} + t_r$. Delay time is defined as the time for collector emitter voltage to fall from V_{CE} to $0.9\,V_{CE}$. V_{CE} is the initial collector emitter voltage. Time t_{dn} may also be defined as the time for the collector current to rise from its initial leakage current I_{CE} to $0.1\,I_C$.



Rise time t_r is the time during which the collector-emitter voltage falls from $0.9V_{CE}$ to $0.1V_{CE}$. It is defined as the time for the collector current to rise from $0.1 I_C$ to its final value I_C. After time t_{on}, collector current I_C and the collector emitter voltage falls to small value called conduction drop $= V_{CES}$ where subscript S denotes saturated value.

Turn off time is of three intervals (i) delay time t_{df}, (ii) initial fall time t_{f1} (iii) final fall time t_{f2}. (ie) $t_{off} = t_{df} + t_{f1} + t_{f2}$.

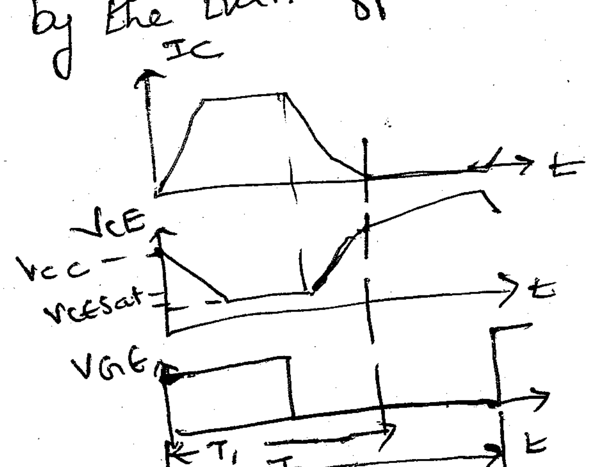
Delay time is the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET}. As V_{GE} falls to V_{GET} during t_{df}, collector current falls from I_C to $0.9I_C$. At the end of t_{df}, collector-emitter voltage begins to rise. The first fall time t_{f1} is defined as the time during which collector current falls from 90 to 20% of its initial value I_C, or the time during which collector-emitter voltage rises from V_{CES} to $0.1V_{CE}$.

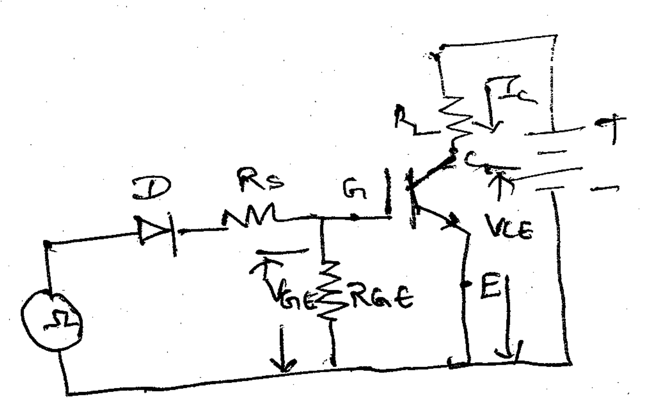
Final fall time t_{f2} is the time during which collector current falls from 20 to 10% of I_C or the time during which collector-emitter voltage rises from $0.1V_{CE}$ to final value V_{CE}.

Conduction and Switching Losses:-

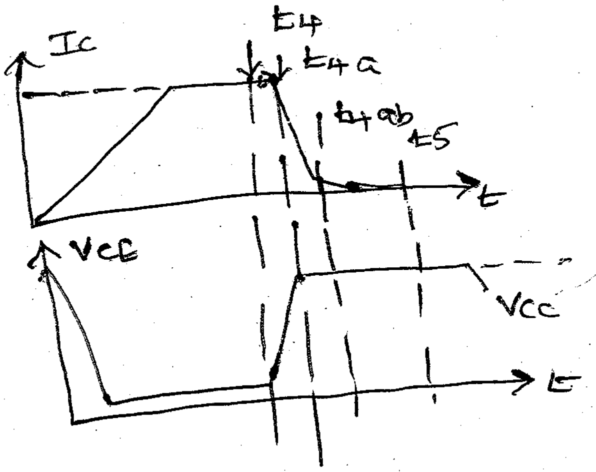
Power losses in the IGBTs will consist of (i) Drive losses (ii) Conduction losses (iii) off state losses, (iv) Switching losses.

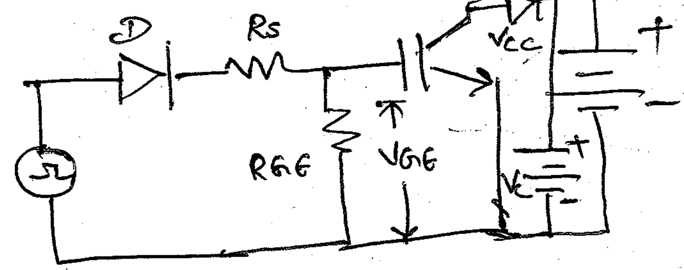
Switching losses can be determined as a function of time, current and voltage. For purely inductive loads, turn-on losses are very small, because the transistor turns on at essentially zero current each cycle. For a purely inductive load, switching losses will be determined by the turn off losses.





Resistive switching





$t_{4a} - t_4 = T_{rv}$
$t_{4b} - t_{4a} = T_{f1}$
$t_5 - t_{4b} = T_{f2}$

Rise time $(T_r) = 0 - t_1$
Turn off delay $(T_d) = t_3 - t_2$
Fall - time two $(T_{f2}) = t_5 - t_4$
Maximum Collector current = I_{cm}

Conduction time $(T_c) = t_2 - t_1$
Fall time one $(T_{f1}) = t_4 - t_3$
Period $(T) = 1/f$.

Collector to emitter Saturation Volts = $V_{CE(sat)}$
Gate to emitter volts = V_{GE}
Collector to emitter power Supply voltage = V_{CC}

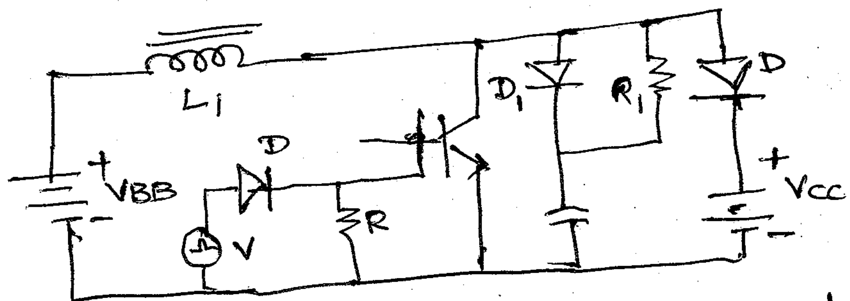
when gate voltage is applied to an IGBT operating in a saturated switching modes, the Collector to emitter voltage decreases and goes into hard saturation if sufficient gate voltage is available. The switching losses are contained in intervals 0 to t_1 and $t_3 - t_4$. The switching power losses are directly proportional to frequency and are independent of duty cycle or pulse width. Conduction losses are proportional to duty cycle D, while off-state losses are proportional to 1-duty cycle.

Gate Drive Circuits:-

It has gate to emitter threshold voltage and a capacitive i/p impedance. In order to turn the device on, the input capacitance must be charged up to a value greater than $V_{GE(th)}$ before collector current can begin to flow. The collector to emitter - Saturation voltage decrease with an increase in magnitude of V_{GE}. Lowest value of on state voltage, V_{GE} should be much greater than $V_{GE(th)}$. To turn off the IGBT a resistor between gate and emitter is all that is required. This resistor provides a path for the gate to emitter input capacitance to discharge.

IGBT has a maximum controllable collector current that is dependent on the gate to emitter dv/dt. That is, higher the gate to emitter turn - off dv/dt, the lower the controllable collector current. The controllable current will dependent on the nature of the load.

Snubbers:-

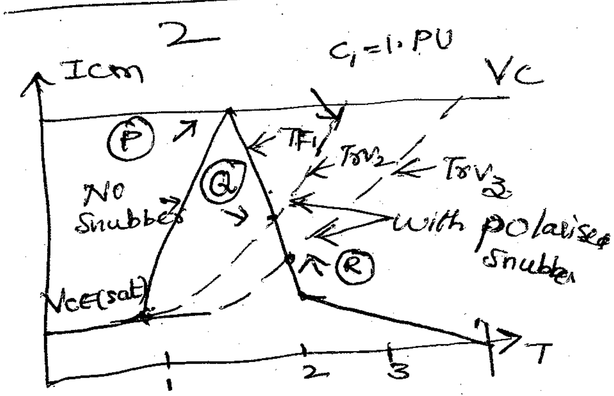


The ability to control the turn on and turn off times by controlling the gate current through appropriate sizing of the series gate resistance further minimizes the need of the turn-on and turn off snubbers. The snubber is used for load line shaping and functions to reduce switching losses within the IGBT. The snubber also reduces turn-off dv/dt to collector to emitter voltage. The controllable current capability is also increased since it varies proportional to V_{CE}. At low values of collector to emitter voltage, controllable collector current is much greater than the specified maximum value.

The switching losses in the IGBT increases significantly due to the presence of T_{f2}. By use of snubbers, device heating is minimized. The operation at point P with no snubber, T_{rv}, T_{f1} and T_{f2}, the IGBT has switching losses equal to

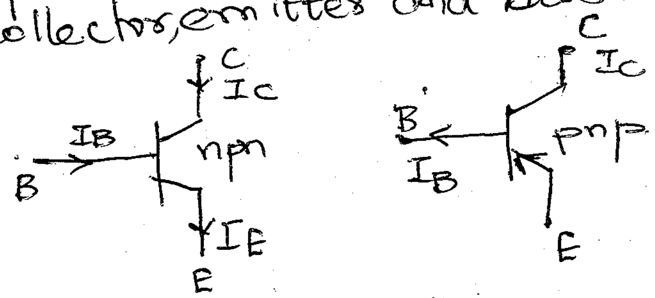
$$P_{av(sw)} = V_{cc} \cdot I_{cm} \cdot f \, \frac{T_{rv1} + 1.1 T_{f1} + 0.1 T_{f2}}{2}$$

When polarised snubber is used the losses are reduced. Snubbering definitely reduces the peak power and average power that the IGBT must dissipate.



Bipolar Junction Transistors:-

It is a three layer, two junction npn or pnp semiconductor device. With one p-region sandwiched by two n-region npn transistor is obtained. The term bipolar denotes that the current flow in the device is due to the movement of both holes and electrons. With two p-region sandwiching one n-region, pnp transistor is obtained. BJT has three terminals collector, emitter and base.

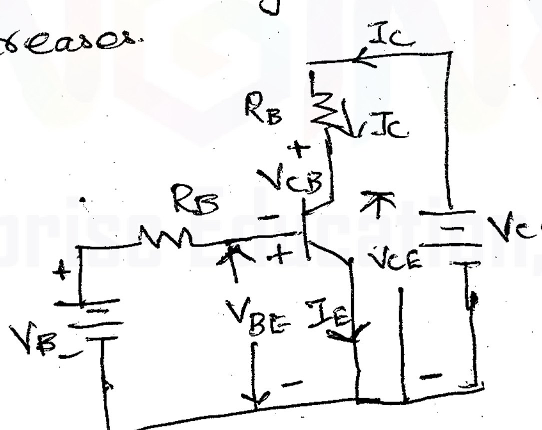


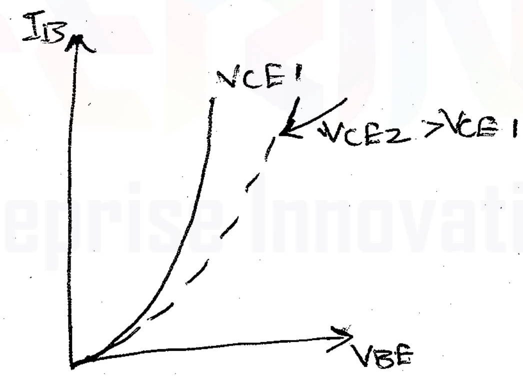
~~Out~~ Common emitter arrangement is more common in switching applications. So npn transistor is used.

Steady state characteristics

Input characteristics:-

A graph b/w base current I_B and base emitter voltage V_{BE} gives input characteristics. When collector emitter voltage V_{CE} is more than V_{CE1}, base current decreases.

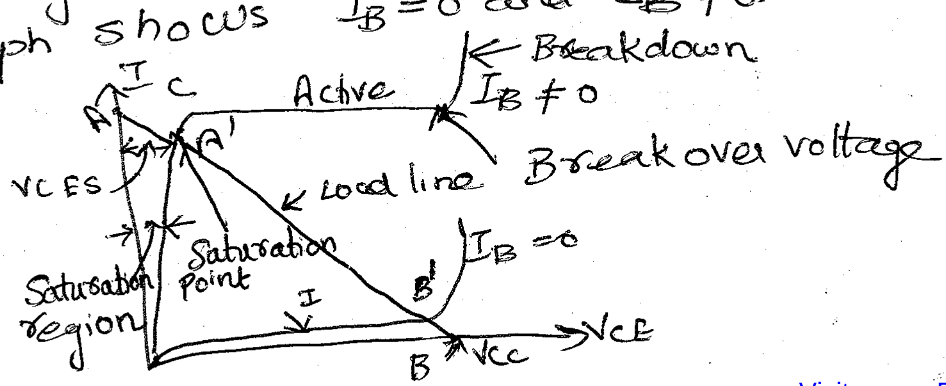




Output characteristics

Graph between collector current I_C and collector emitter voltage V_{CE} gives output characteristics of a transistor. For base current to be zero $I_b = 0$, V_{CE} is increased, a small leakage current flows. As the $I_B \uparrow$, $I_C \uparrow$.

The graph shows $I_B = 0$ and $I_B \neq 0$.



The low voltage V_{CE} is called saturation region. In this region transistor acts like a switch. The curve 2 indicates by increasing V_{CE} and almost constant I_C is the active region. In this region transistor acts like an amplifier. The vertical rising curve is the breakdown region.

The collector current I_C is given by

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}.$$

A load line AB is the locus of all possible operating points. When transistor is on, V_{CE} is zero and $I_C = V_{CC}/R_C$. shown by point A. When transistor is off, V_{CC} appears across collector emitter terminals and there is no collector current. Shown by point B.

Relation between α and β:-

$$\alpha = \frac{I_C}{I_E}$$ is called forward current gain.

Also $I_C < I_E$ α varies from 0.95 to 0.99.

Base current is effectively the input current and collector current is the output current. The ratio of collector current I_C to base current I_b is known as the current gain β.

$$\beta = \frac{I_C}{I_B} = h_{fe}.$$

Using KCL, $I_E = I_C + I_B$.

$I_E >$ all the three current.

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \beta = \frac{\alpha}{1-\alpha}$$

$$\boxed{\alpha = \frac{\beta}{\beta + 1}}$$

Transistor switch:-

Transistor operates either in saturation region or cutt off region. For Ideal switch, point A is in Saturated state as ~~cotto~~ closed switch with $V_{CE}=0$, point B in cut off state with open switch $I_C=0$. Large base current will cause transistor to work in saturation region at point A' with V_{CES} small voltage. V_{CES} is the on-state voltage drop of order 1V. when $I_b=0$, transistor is turned off, so operation shift to B', in cut off region.

Apply KVL

$$V_B - R_B I_B = -V_{BE} = 0$$

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

$$= V_{CC} - \frac{\beta R_C}{R_B}(V_B - V_{BE})$$

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE}$$

V_{CES}, Collector emitter saturation voltage.

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C}$$

$$I_{BS} = \frac{I_{CS}}{\beta}.$$

With $I_B > I_{BS}$, hard drive transistor is obtained. V_{CES} become low and on state losses of transistor are reduced.

The ratio of I_B to I_{BS} is overdrive Factor (ODF)

$$ODF = \frac{I_B}{I_{BS}}.$$

Ratio of I_{CS} to I_B is called forward current gain β_F.

$$\beta_F = \frac{I_{CS}}{I_B}.$$

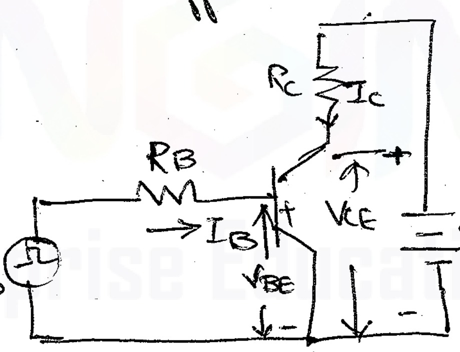
The total power loss $P_T = V_{BE} I_B + V_{CE} I_C$.

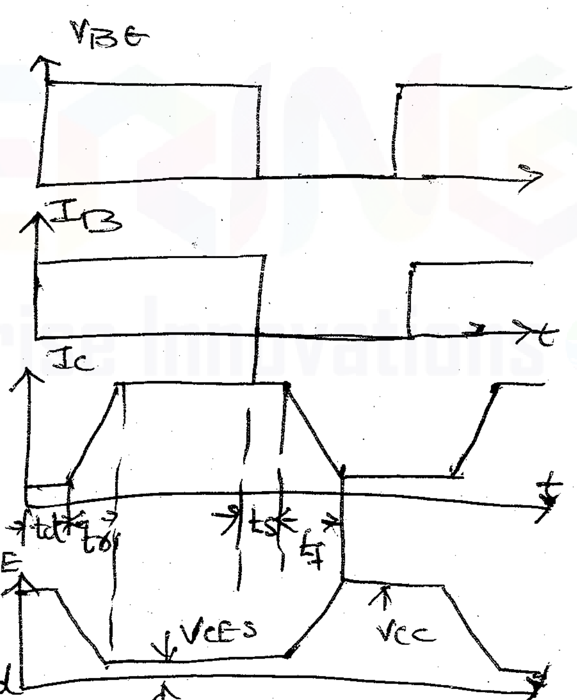
Transistor Switching performance

A transistor cannot be turned on instantly because of the presence of internal capacitance. When V_{BE} is applied, $I_B \uparrow I_{BS}$, I_C increases to collector leakage current I_{CEO} or zero. At delay time t_d the collector current begins to rise. This delay is due to the time required to charge base emitter capacitance to $V_{BES} = 0.7V$. After time delay, I_C rises to steady state I_C which is known as rise time t_r. So $t_{on} = t_d + t_r$.

When V_{BE} is removed at t_1, collector current does not change for a time t_s called storage time. During t_s, charge is removed from base. At time t_s, I_C falls, V_{CE} starts building up. After time t_f, fall time I_C decreases to I_{CEO}. V_{CE} rises to V_{CC}.

So turn off time $t_{off} = t_s + t_f$.

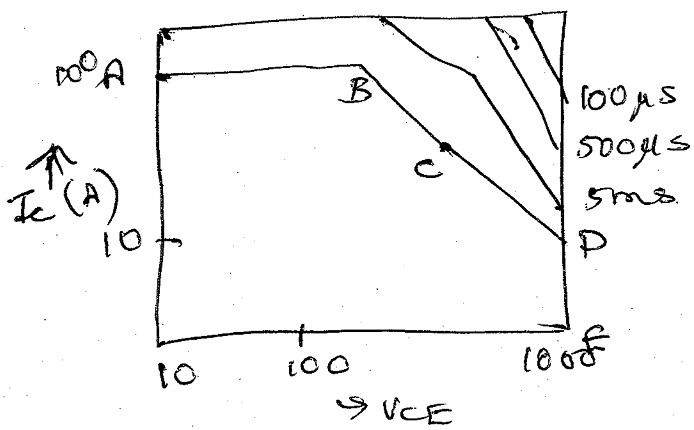




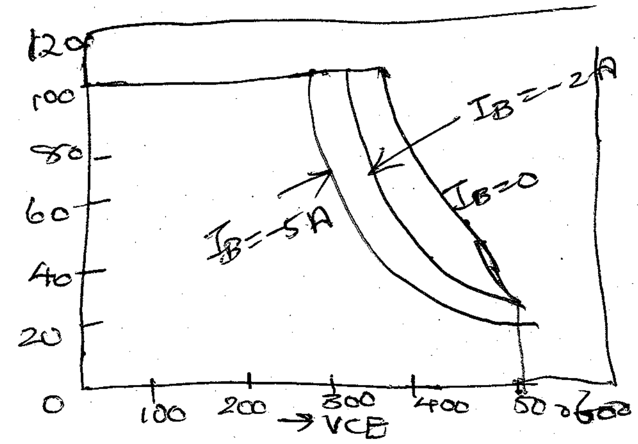
Safe operating Area: (SOA)

Two types of SOA are FBSOA and RBSOA.

FBSOA: when base emitter junction is forward biased to turn on the transistor. Boundary AB is the maximum limit for dc and continuous current for $V_{CE} < 80V$. For $V_{CE} > 80V$, I_C reduces to BC to limit the junction temperature. For higher V_{CE} current should be reduced to avoid secondary breakdown. CD is secondary breakdown. DE gives maximum voltage capability for this transistor.



FBSOA



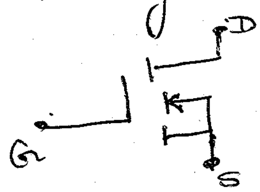
RBSOA.

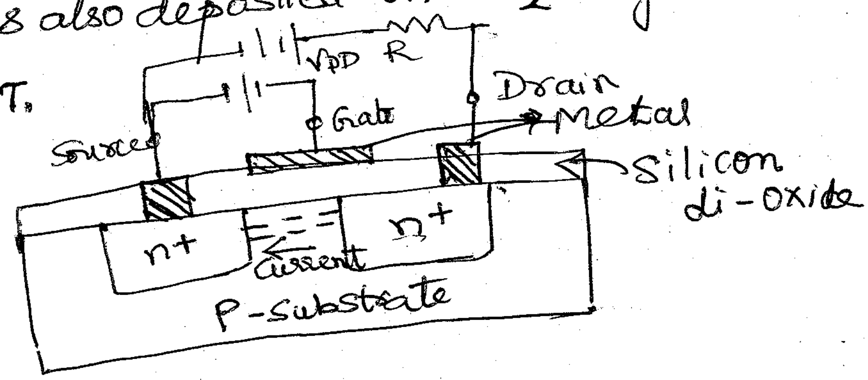
During turn off, a transistor is subjected to high current and high voltage with base emitter junction reverse biased. SOA for turn off is specified as reverse blocking safe operating area (RBSOA). The graph is of I_c Vs V_{CE}. With increased R.B, RBSOA decrease in size

Power MOSFET:-

* It has three terminals drain Source and gate.
* BJT is a current Controlled device whereas MOSFET is a voltage Controlled device. Operation depends on the flow of majority carriers only. MOSFET is a unipolar device. The Control Signal required to trigger the MOSFET will be more when compared to BJT.
* Gate circuit impedance in MOSFET is high of the order of 10^9 ohm.
* BJT suffers from second breakdown voltage, whereas MOSFET is free from this problem. MOSFET is finding applications in low power high frequency converters.
* MOSFETs are of two types:- n channel Enhancement MOSFET and p-channel enhancement MOSFET. n-channel MOSFET is more common because of higher mobility of electrons.

On p-substrate two heavily doped n^+ regions are diffused. An insulating layer of silicon dioxide is grown on the surface. Now the insulating layer is etched in order to embed metallic source and drain terminals. A layer of metal is also deposited on SiO_2 layer to form the gate of MOSFET.

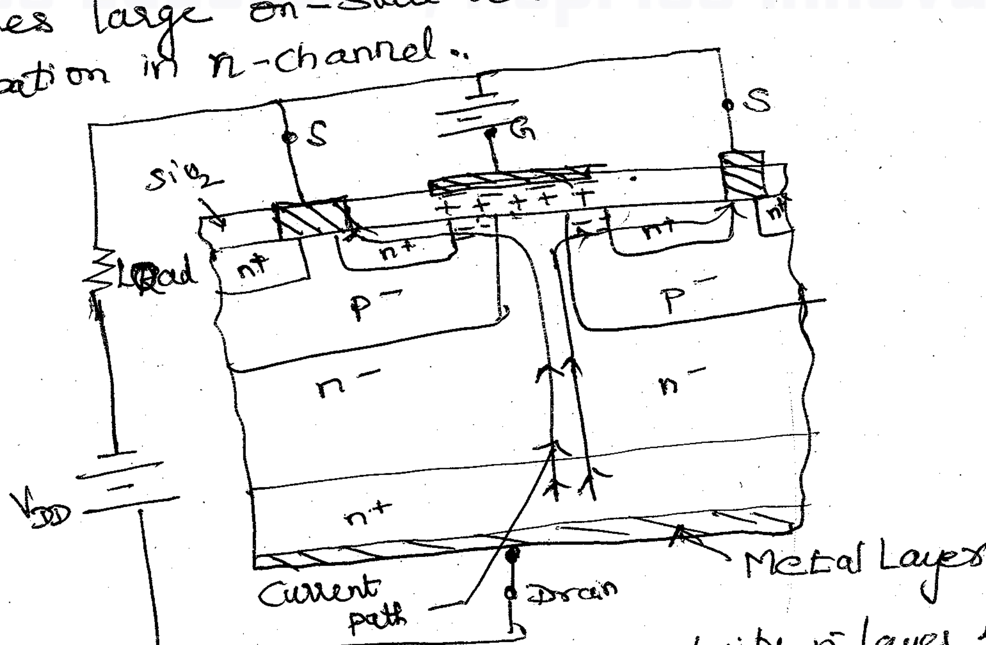




When gate is open, no current flows from drain to source and load because of one reverse-biased n^+-p junction. When gate is made positive with respect to source, an electric field is established as shown.

If V_{GS} is +ve, n channel becomes more deep and therefore more current flows from D to S. The drain current I_D is enhanced by gradual increase of gate voltage, hence enhancement MOSFET.

Disadvantage: Conducting n-channel in between drain and source gives large on-state resistance. This leads to high power dissipation in n-channel.



n^+ substrate, high resistivity n^- layer is epitaxially grown. The thickness of n-layer determines the

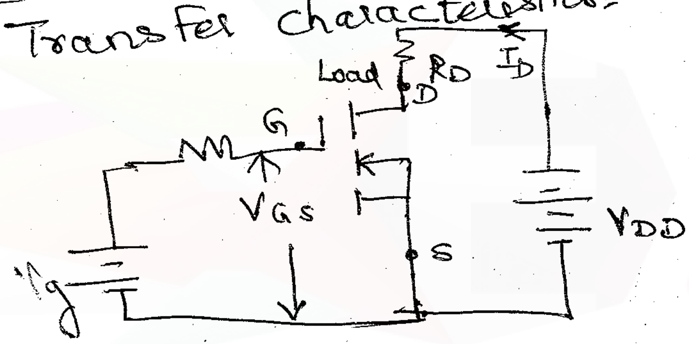
Voltage blocking capability of the device. A metal Layer is deposited to form the drain terminals. Now p^- regions are diffused in the epitaxially grown n^- Layer.

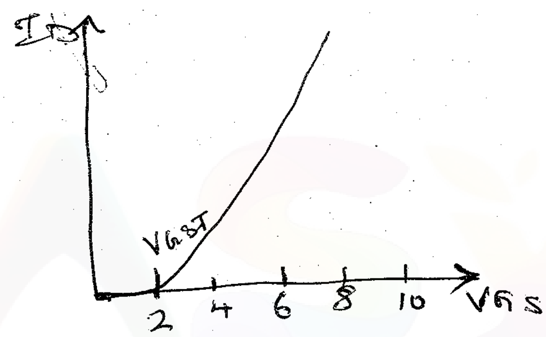
When gate circuit voltage is zero, V_{DD} is present, n^--p^+ junctions are reverse biased and no current flows from drain to Source. When gate terminal is made positive with respect to source, an electric field is estabilished and electrons form n-channel in the p-region.

Power MOSFET is due to majority carriers.

MOSFET characteristics:

(a) Transfer characteristics:

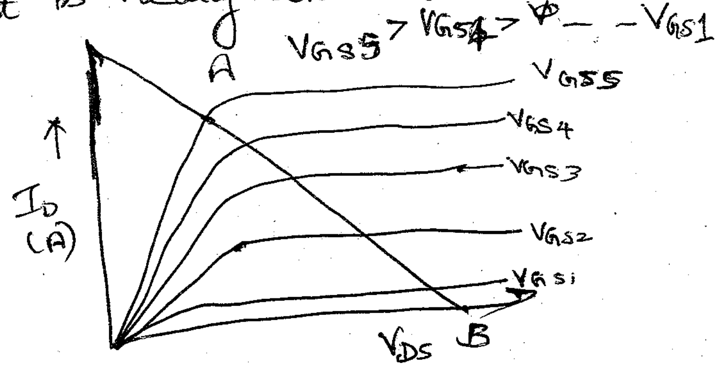




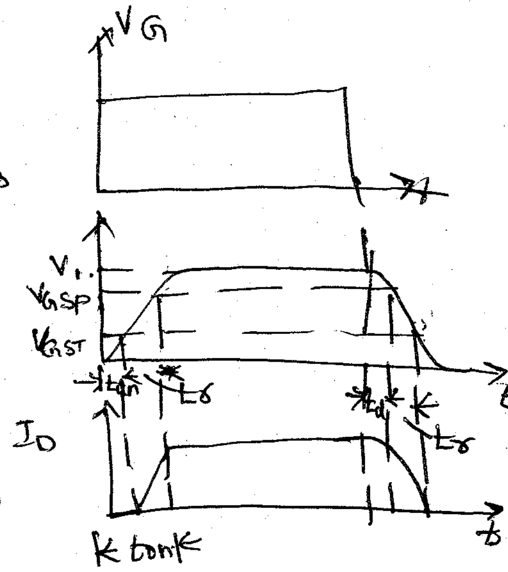
There is threshold voltage V_{GST} below which the device is off. The magnitude of V_{GST} is of the order of 2 to 3V.

(b) O/P characteristics:

Power MOSFET indicate the variation of drain current I_D as a function of drain-source voltage V_{DS}. For low value of V_{DS}, the graph between $I_D - V_{DS}$ is almost linear, this indicate a constant value of on-resistance $R_{DS} = V_{DS}/I_D$. For given V_{GS}, if V_{DS} is increased, output characteristics is relatively flat indicating that drain current is nearly constant.



Switching Characteristics:-



At turn on, there is an initial delay t_{dn} during which i/p capacitance charges to gate threshold voltage V_{GST}. t_{dn} is called turn on delay time.

t_r called rise time, which gate voltage rises to V_{GSP}, a voltage sufficient to drive the MOSFET into on state. During t_r, drain current rises from zero to full on current I_D. Total turn on time $t_{on} = t_{dn} + t_r$.

Turn on time is reduced by low impedance gate drive source.

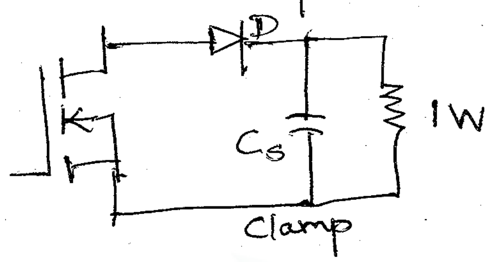
MOSFET is a majority carrier device, turn off process is initiated soon after removal of gate voltage at time t_1. The turn off delay t_{df} is the time during which i/p capacitance discharges from overdrive gate voltage V_1 to V_{GSP}. The fall time t_f is the time during which i/p capacitance discharges from V_{GSP} to threshold voltage. During t_f, I_D falls to zero.

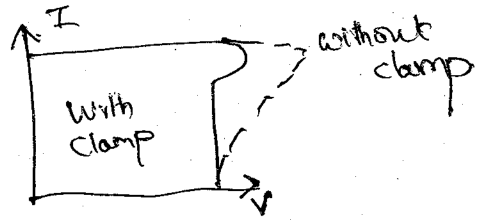
Comparison of MOSFET with BJT

1. MOSFET has lower switching losses but on-state resistance and conduction losses are more. BJT has higher switching losses but lower conduction loss.
(ii) MOSFET is voltage controlled device, BJT is current controlled device.
(iii) MOSFET has positive temperature coefficient for resistance so ||el operation is easy. BJT has negative temperature coefficient, so current sharing resistors are necessary during parallel operation of BJTs.
iv) In MOSFET, secondary breakdown does not occur, because it has positive temperature coefficient. BJT has negative temperature coefficient so secondary breakdown occurs.
v) MOSFET in high voltage ratings have more conduction loss.
vi) MOSFET is available in 500V, 140A whereas BJT in 1200V, 800A.

Safe operating Area of MOSFET:-

The SOA of a power MOSFET is much better than that of a bipolar. The MOSFET, being a majority carrier device, has a positive temperature coefficient of resistance, and is immune from the hot-spot formation and second breakdown phenomenon that plague the bipolar transistor. MOSFET are therefore generally much more rugged than bipolar and snubber clamp circuitry can be smaller and less dissipative.



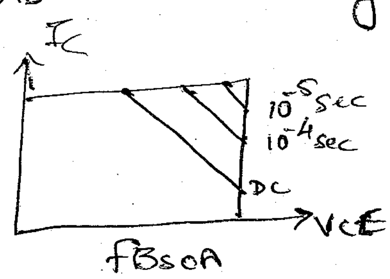


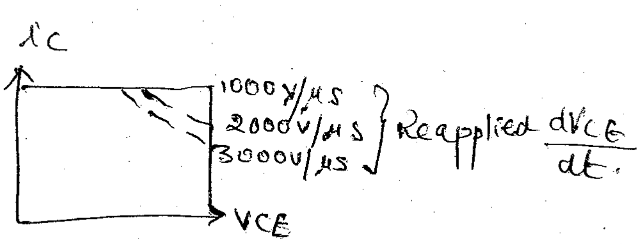
Advantages

1. Overload and peak current handling capability are high. MOSFET are generally much more rugged and forgiving than bipolars.
2. Absence of second breakdown reduces snubber circuitry in switching applications and gives more power handling capability in linear application.
3. Leakage current is relatively low, typically in the order of nanoamperes.

Safe operating Area of IGBT:-

FBSOA is square for short switching times, identical to the power MOSFET. For longer switching FBSOA behaviour of the IGBTs are thermally limited.





The RBSOA is somewhat different than FBSOA. The upper right hand corner of RBSOA is progressively cut out and the RBSOA becomes smaller as the rate of change of reapplied collector to emitter voltage dV_{CE}/dt becomes larger. By proper choice of V_{GE} and gate drive resistance, the device user can control the reapplied dV_{CE}/dt.

The breakdown voltage of PNP transistor sets the maximum permissible Collector-emitter voltage. The beta of the PNP transistor is quite low, so its breakdown voltage is essentially BV_{CBO}, the breakdown voltage of the drift body junction. A desirable feature of IGBT is the on-state voltage $V_{CE(on)}$ varies very little between room temperature and maximum temperature. IGBT has flat temperature characteristics because of positive and negative temperature coefficient.

Applications of IGBT:

Used in Dc and ac motor drives, UPS systems, power supplies and drives for solenoids, relays & contactors.

IGBT's are becoming popular because of lower gate drive requirements, lower switching losses and smaller snubber circuit requirements.

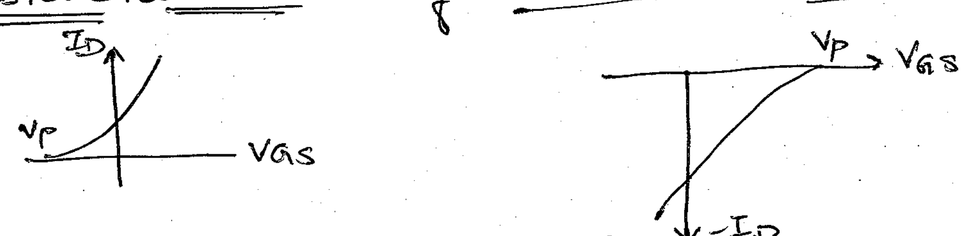
IGBT are less size, with a range of 1200V, 500A.

Steady state characteristics of MOSFET:

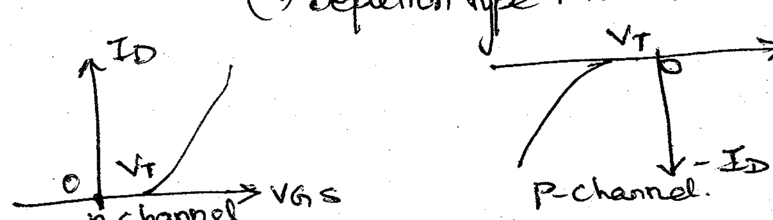
MOSFET is a voltage controlled device which have high i/p impedance, since gate draws a very small leakage current on the order of nano amperes. Current gain $\alpha = \frac{I_D}{I_G}$ of order of 10^9.

Transconductance $g_m = \frac{I_D}{V_{GS}}\Big|_{V_{DS}\ \text{constant}}$

Transfer characteristics: of n-channel and p-channel MOSFET



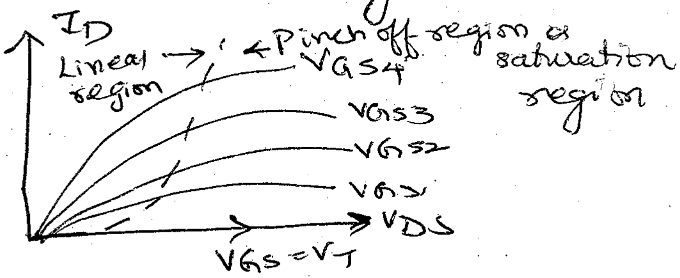
(a) Depletion type MOSFET



b) Enhancement type MOSFET

The o/p characteristics of n-channel has three regions of operation (1) Cut off region where $V_{GS} < V_T$ (2) Pinch off or Saturation region $V_{DS} \geq V_{GS} - V_T$ (3) linear region $V_{DS} \leq V_{GS} - V_T$. The pinch off occurs at $V_{DS} = V_{GS} - V_T$. In linear region the I_D ↑ in proportions to V_{DS}.

Due to high drain current and low drain voltage, MOSFET are operated in linear region for switching actions.
In Saturation region I_D remains constant for increase in value of V_{DS} and transistors are used in this region for voltage amplifications.



The o/p resistance $r_o = R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D}$
which is very high in pinch of region of megaohms and small in linear region of milliohms.
For depletion type MOSFET the gate voltage could be either positive or negative.
Enhancement type MOSFET respond to a positive gate voltage only.

<u>What happens when gate source voltage is negative (or) why negative Voltage is not applied to MOSFET</u>

If V_{GS} is −ve, some of the electrons in n-channel area are repelled and a depletion region is created below the oxide layer, resulting in a narrower effective channel and a high resistance from the drain to source R_{DS}. and no current flow from drain to source $I_{DS} = 0$. This is called pinch off voltage V_P.

When V_{GS} is +ve, the channel becomes wider and I_{DS} ↑ due to reduction in R_{DS}.

GTO (Gate turn off)

* GTO can be turned on by applying a short Positive gate signal and turned off by negative short gate signal.
* It is a nonlatching device.

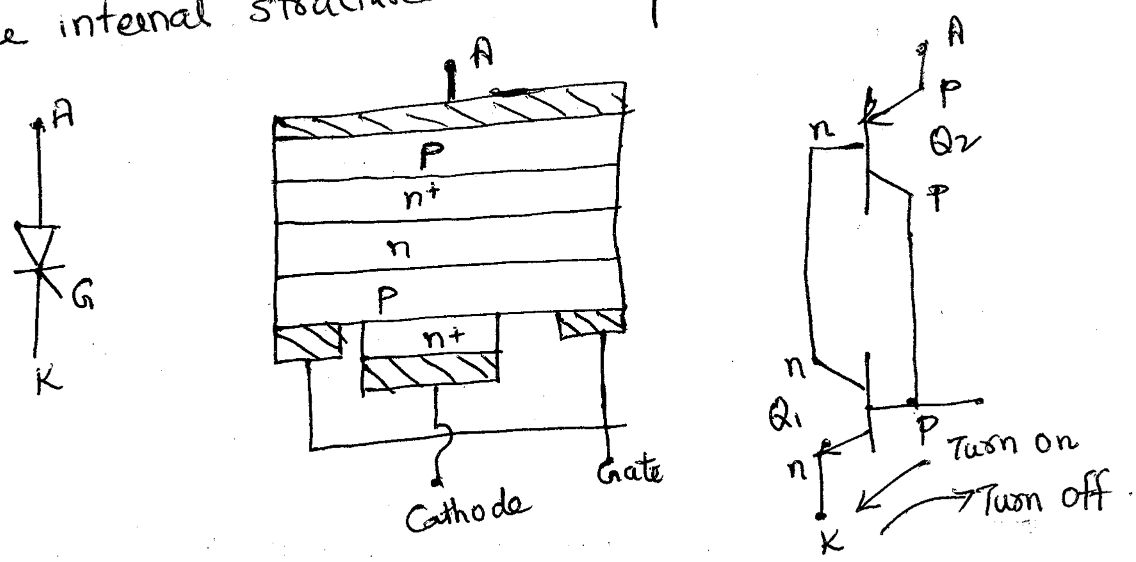
Advantages of GTOs over SCR.

1) Elimination of Commutating components in Forced Commutation. results in cost, weight and Volume to be less
2) Reduction in acoustic and electromagnetic noise due to the elimination of Commutation Chokes
3) Faster turn off
4) Improved Efficiency.

Advantages of GTOs over BJT in low power applications:-

1) Higher blocking voltage capability
2) High ratio of peak controllable current to average current
3) High ratio of peak surge current to average current.
4) High on state gain.
5) GTO is a latch on device and latch off device.

The internal structure and equivalent circuit is shown.

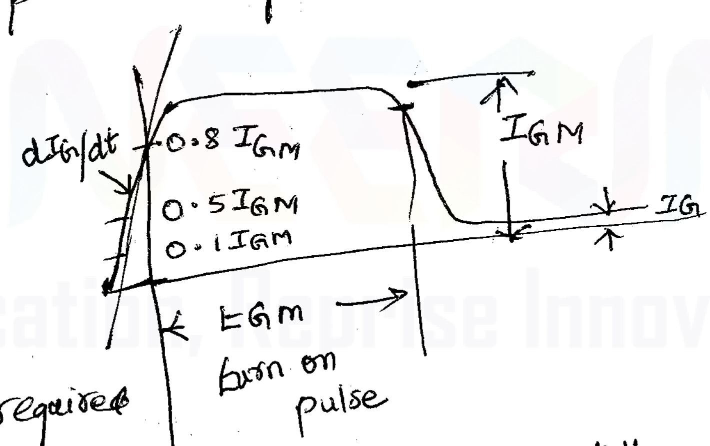


* Compared to thyristor, it has an additional n^+ layer near the anode that forms a turn off circuit between gate and cathode in parallel with the turn on gate.

* A large pulse current is passed from cathode to gate to take away sufficient charge carriers from the cathode (ie) emitter of npn transistor Q_1
* PNP transistor can be taken for regenerative action.
* Q_1 turns off, Q_2 is left with an open base, GTO returns to non conducting state.

Turn on:-

* GTO has a highly interdigited gate structure with no regenerative gate
* A large gate pulse is required to turn on GTO.



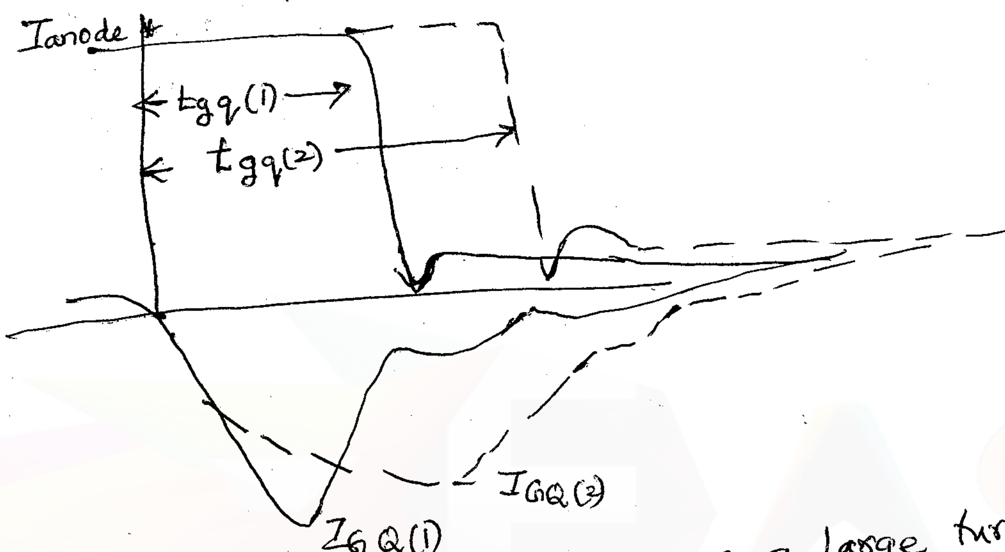
* The rate of rise of gate current dig/dt affects the device turn on losses
* A longer period is required if the anode current di/dt is low. to maintain I_{GM} constant until anode current stabilizes.

On state:

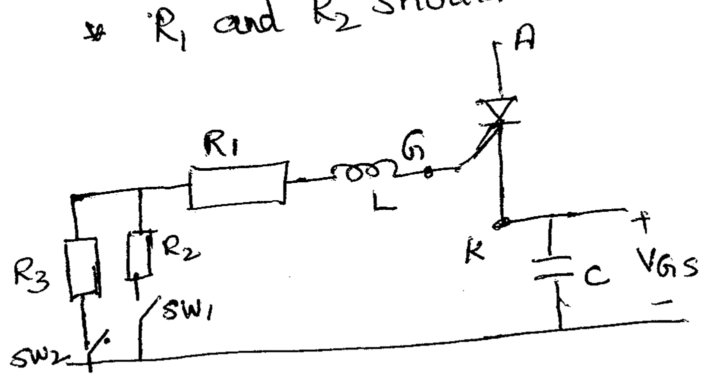
* Forward gate current has to been given continuously for whole conduction period.
* Otherwise device does not remain in On state period
* On state gate current should be atleast 1% of turn on pulse to ensure that gate does not unlatch.

Turn off:

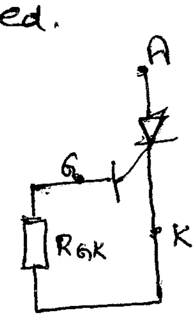
* Process involves the extraction of the gate charge, gate avalanche period and the anode current decay.
* The initial peak turn off current and turn off time depend on the external circuit components.



* Since GTO requires a large turn off current a charged capacitor is used to provide the required turn off gate current.
* Inductor L limits the turn off di/dt of the gate current through the circuit formed by R_1, R_2, SW_1 and L.
* V_{GS} should be selected to give the required value of V_{GQ}.
* R_1 and R_2 should be minimized.



Turn off circuit



Gate cathode resistance R_{GK}.

* GTO to be reverse biased by keeping SW_1 closed during the whole off state period. or using a higher impedance circuit SW_2 and R_3, provided a minimum negative voltage exists.

* ~~High~~ High impedance SW_2 and R_3 must sink gate leakage current.

* In case of failure of auxillary supplies for gate turn off circuit, minimum gate cathod resistance (R_{GK}) should be applied to make the device in reverse biased.

* GTOs are used in voltage source converters where a fast recovery anti parallel diode is required across each GTO.

* GTO do not need reverse voltage capability. Such GTOs are asymmetric GTOs.

Dc - DC Chopper

The Conversion of fixed dc Voltage to an adjustab dc output voltage, through the use of semiconductor devi Can be carried out by the use of two types of dc to d Conversion. Ac link chopper and Dc link Chopper

Ac link chopper:

Dc is first Converted to ac by inverter. is then stepped up or stepped down by a transformer wh is then converted back to dc by a diode rectifier. The Conversion is in two stages, dc to ac and then ac to d ac link chopper is costly, bulky and less efficient.

DC chopper:

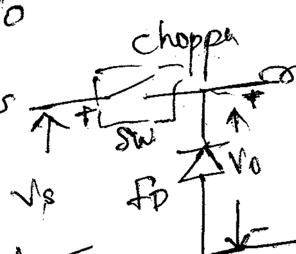
It is a static device that converts fixed dc i/p Voltage to a variable dc o/p voltage directly. chopper are now being used all over the world for rapid transis System. These are also used in trolley cars, marine hoi for lifts trucks and mine haulers. The future electric autom are likely to use choppers for their speed control and brakin chopper systems offer smooth control, high efficiency, fast response and regeneration.

PRINCIPLE OF chopper operation:

It is a high speed on/off semiconductor switc It connects source to load and disconnects the load from Source at a fast speed. The chopper is represented by a Switch SW inside a dotted rectangle which may be turned on or turned off. During the period Ton, chopper is and load voltage is equal to source voltage Vs. During the interval Toff chopper is off, load current flows through the freewhe diode FD. As a result, load terminals are short circuited by FD and load Voltage is therefore zero during Toff. A chopper dc voltage is produced at the load terminals. The load curren is continuous.

The average load voltage Vo

$$V_0 = \frac{T_{on}}{T_{on}+T_{off}} V_s = \frac{T_{on}}{T} V = \alpha V_s$$



T_{on} - on - time; T_{off} - off - time

$T = T_{on} + T_{off}$ - chopping period

$\alpha = \frac{T_{on}}{T}$ = duty cycle

The load is independent of ...

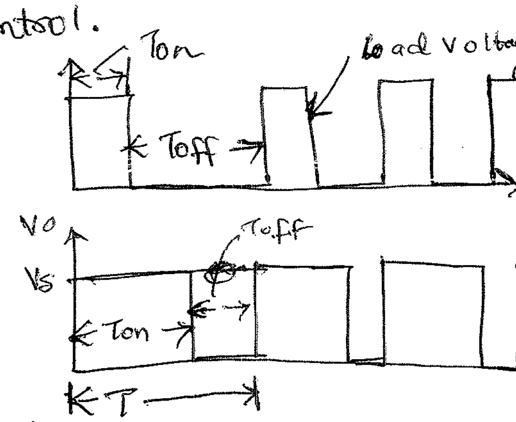
$V_0 = f\, T_{on} \cdot V_s$

$f = \frac{1}{T}$ = chopping frequency.

Control strategies:-

Constant frequency System

The on time Ton is varied but chopping frequency constant. Variation of Ton means adjustment of pulse width ... is also called pulse width modulation scheme. This has been referred as time ratio control.

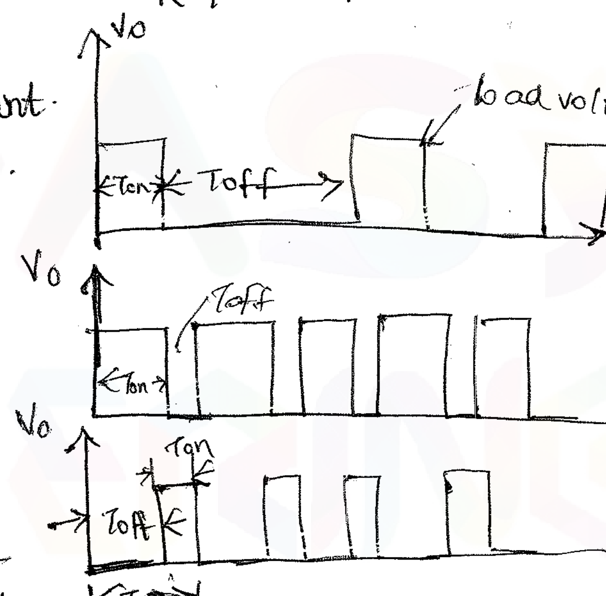


$T_{on} = \frac{1}{4} T$ so that $\alpha = 0.25$ $\alpha = 25\%$.

$T_{on} = \frac{3}{4} T$ so that $\alpha = 0.75$, or $\alpha = 75\%$

Variable frequency System:-

Chopping frequency is varied and on time (i) Ton is kept constant.
(ii) off time Toff is kept constant.
This method of controlling α is also called frequency modulation scheme.



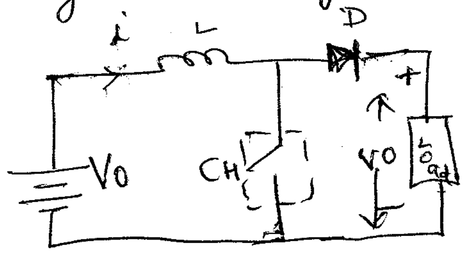
These are under
(i) Chopping frequency has to be varied over a wide range for the control of o/p voltage in frequency modulation.
(ii) For the control of α, frequency variation would be wide. possibility of interference with signalling and telephone ... frequency modulation scheme.
(iii) The large off time in frequency modulation scheme make the load current discontinuous which is undesi...

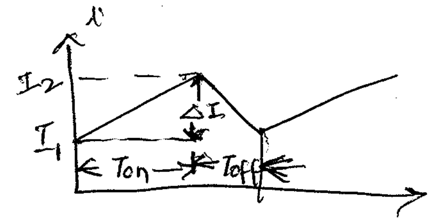
Current limit Control:-

In Current limit Control strategy, the chopp... is switched ON and OFF so that the current in the loa... is maintained between two limit. when current exceeds upper l... the chopper is switched off. During off period, the load current fre... and decreases exponential. When it reaches lower limit the chopper is ... Current limit is possible with constant frequency or with constant ...

Step up Chopper:

$V_0 < V_s$, so therefore it is called step-down chopper.
Average o/p voltage $V_0 > V_s$ it is called stepup Chopper!





A Large inductor L in series with Source voltage V_s. When the chopper CH is on, the closed path is shown. The inductor stores energy during Ton period. When the chopper CH is off inductor current cannot die down instantaneously, this current is forced to flow through the diode and load for a time Toff. As the current tends to decrease, polarity of emf induced in L is reversed. So load voltage $V_0 = V_s + L\left(\frac{di}{dt}\right)$.

When CH is on, current through the load would increase from I_1 to I_2.
When CH is off, current would fall from I_2 to I_1.
With CH on, Source voltage is applied to L (ie) $V_L = V_s$.
With CH on, $V_L - V_0 + V_s = 0$ or $V_L = V_0 - V_s$.
Here V_L = Voltage across L.

The energy input to inductor from the source, during the period Ton is

$$W_{in} = (\text{Voltage across } L)(\text{average current through } L)\,T_{on}$$

$$= V_s\left(\frac{I_1 + I_2}{2}\right)T_{on}.$$

During the time Toff, when chopper is off, energy released by inductor to the load is

$$W_{off} = (\text{Voltage across } L)(\text{average current through } L)\,T_{off}$$

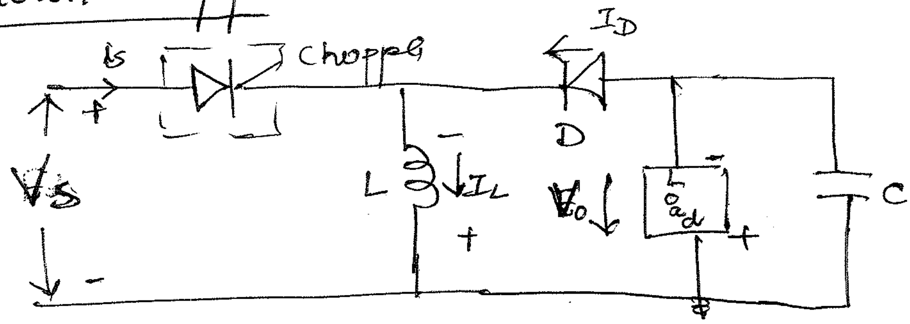
$$= (V_0 - V_s)\left(\frac{I_1 + I_2}{2}\right)T_{off}$$

$$V_0 = V_s\frac{T}{T - T_{on}} = V_s\frac{1}{1-\alpha}.$$

for $\alpha = 0$ $V_0 = V_s$, $\alpha = 1$ and $V_0 = \infty$

When chopper is turned on and off, so that α is variable and the required step up average o/p voltage, more than source voltage is obtained.

Step down chopper:



When the chopper is on, the supply current flows through V_S^+ - CH - L - V_S^-. Hence the inductor L stores the energy during the Ton period.

When the chopper CH is off, the inductor current tends to decrease and as a result, the polarity of emf is induced in L is reversed. Thus the inductance energy discharges in the load through the path.

L_+ - Load - D - L^-

During Ton, the energy stored in inductance $W_i = V_S I_S T_{on}$

During Toff, energy fed to load is $W_o = V_o I_S T_{off}$.

For steady state

Input energy W_i = Output energy W_o

$$V_S I_S T_{on} = V_o I_S T_{off}$$

$$V_o = V_S \frac{T_{on}}{T_{off}}$$

$$V_o = V_S \frac{T_{on}}{T - T_{on}} = V_S \frac{1}{\frac{T}{T_{on}} - 1}$$

$$V_o = \frac{V_S}{\frac{1}{\alpha} - 1}$$

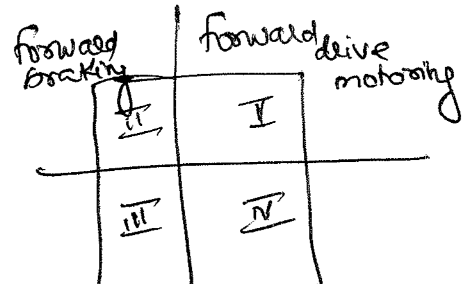
$$\boxed{V_o = V_S \frac{\alpha}{1-\alpha}}$$

$\alpha < 0.5$ step up chopper

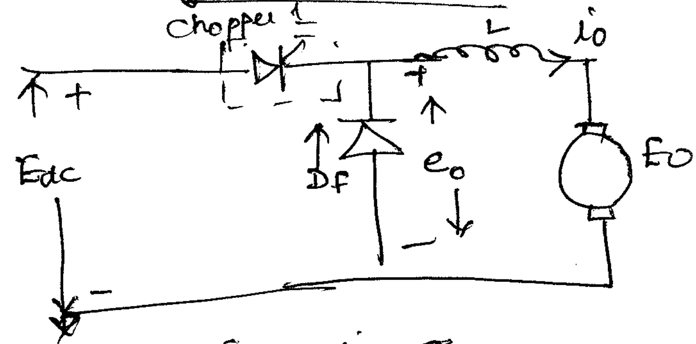
$\alpha > 0.5$ step down

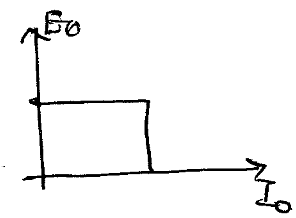
Chopper Configuration:

If the load is a seperately excited motor of constant field, then positive voltage and positive current in first quadrant give rise to forward drive. Changing the polarity of armature voltage and armature current results in a reverse drive in III^rd quadrant. In II and IV quadrant the direction of energy flow is reversed and the motor operates as a generator braking rather than driving



First quadrant or Type A chopper

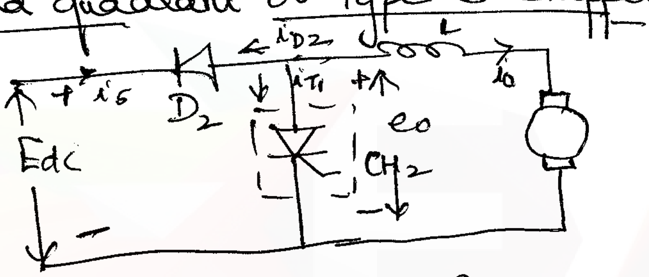


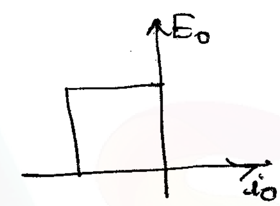


when CH is on $e_0 = E_{dc}$ ~~$i_0 = 0$~~

when CH is off $e_0 = 0$ current i_0 flows in the same direction [through] Freewheeling diode D_F. Both average load Voltage and I_0 are positive so power flows from source to load. Average o/p vo[ltage] is less than dc i/p voltage E_{dc}. This is also called stepdown cho[pper]

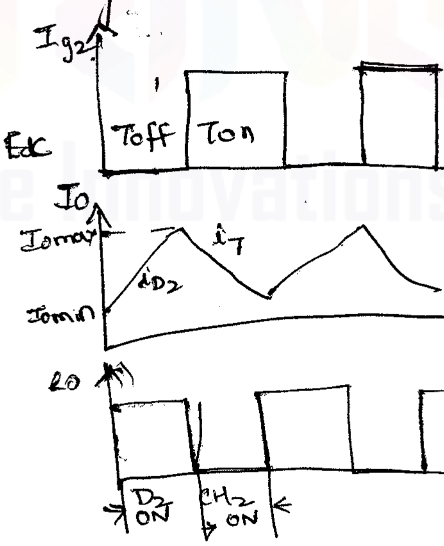
Second quadrant or Type B chopper





when CH_2 is on $e_0 = 0$

when CH_2 is off diode D_2 conducts $e_0 = E_{dc}$. Average load voltage is positive and load current is negative. Since power flow from Power flows from load to Source. [...] from load of lower voltage e_0 to higher voltage E_{dc}. This is also called step up chopper. This configuration is used [for] regenerative braking of dc motors.



for interval $0 < t < T_{off}$ diode D_2 conducts $e_0 = E_{dc}$

$$L\frac{di_0}{dt} + Ri_0 = E_{dc} - E_b$$

$$\frac{di_0}{dt} + \frac{R}{L} i_0 = \frac{E_{dc} - E_b}{L}$$

$$I_0(t) = \left(\frac{E_{dc} - E_b}{R}\right)\left(1 - e^{-t/\tau}\right) + I_{omin}\, e^{-t/\tau}$$

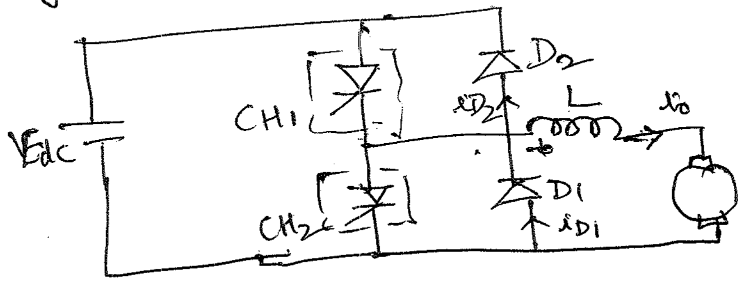
$$I_{omax} = \left(\frac{E_{dc} - E_b}{R}\right)\left(1 - e^{-T_{off}/\tau}\right) + I_{omin}\, e^{-T_{off}/\tau}$$

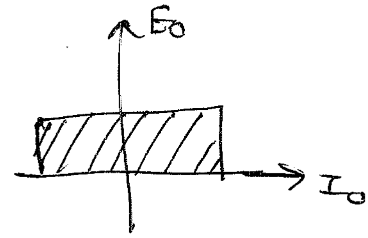
At $t = T_{off}$, CH_2 is turned [on] $e_0 = 0$ $i_0 = I_{max}$.

for $T_{off} < t < T$ $\quad \frac{di_0}{dt} + \frac{Ri_0}{L} = \frac{-E_b}{L}$

$t' = t - T_{off}$

Type C Chopper or Two Quadrant Chopper





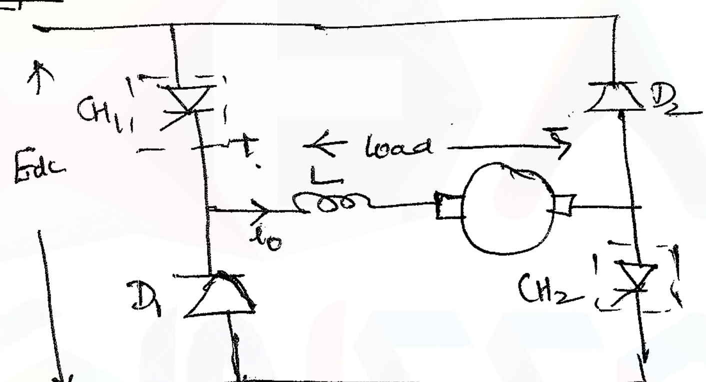
CH1 and D1 Conducts for the 1st quadrant, CH2 D2 conduct
second quadrant converter.

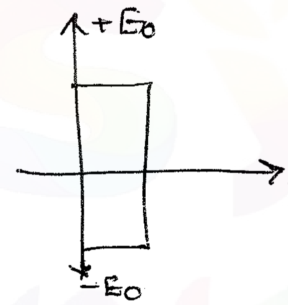
$e_0 = e_{dc}$ when CH1 or Diode D2 Conducts.

CH1 is turned off inductance L forces the load current
flow through diode D1 till the value of $L\frac{di_s}{dt}$ becomes equal
the back emf of the load and i_0 becomes zero.

When CH2 is turned on. $e_0 = 0$, the load current flows in
reverse direction.

Type D chopper

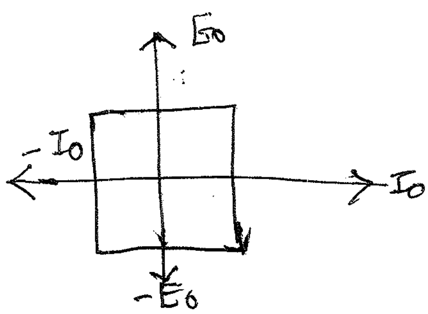


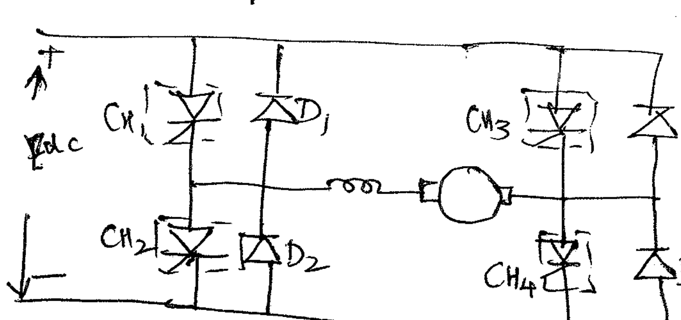


When CH1 and CH2 the current flows through Vdc - CH1 - L - C
During this period D1 and D2 are turned off.
When CH2 is turned off, D2 starts conducting and the load c
freewheels through the load.

When both CH1 and CH2 OFF D1 and D2 Conducts provides t
path for the load current to flow back to Supply.

Type E chopper or Four Quadrant chopper:-





When CH_1 and CH_4 are turned on, current flows through E_{dc} – CH_1 – loa
E_0 and I_0 are positive in 1st quadrant operation.
When both choppers CH_1 and CH_4 are turned off, load dissipate
its energy through the path D_3 – E_{dc+} – E_{dc-} – D_2 – load.
E_0 is –ve, I_0 +ve, and fourth quadrant operation is possi
When CH_2 and CH_3 are turned on, current flows through
E_{dc+} – CH_3 – load – CH_2 – E_{dc-}. Both I_0 and E_0 are negative
in Third quadrant.
When CH_2 and CH_3 are turned off, load dissipates its en
through the path load – D_1 – E_{dc+} – E_{dc} – D_2 – load.
E_0 is positive, I_0 is negative, and second quadrant opera
So four quadrant chopper configuration can be used for a
reversible regenerative dc drive.

First quadrant:
CH_4 is ON, CH_3 off and CH_1 is operated. With CH1, CH4 on, V_0
and i_0 begins to flow. V_0 & I_0 are positive giving 1st Quadrant ope
CH1 is turned off, positive current freewheels through CH_4, D_2.

Second quadrant: CH_2 is operated, CH1, CH_3 and CH_4 are off. With
CH_2 on, reverse current flows through L, CH_2, D_4 and E. Inducta
L stores energy during the time CH_2 is on.
CH_2 → turned off current is fed back to source throug
diode D_1, D_4. Here $E + L\frac{di}{dt}$ is more than source voltage. V
V_0 is positive, I_0 is –ve and it is second quadrant operati
of chopper. So power is fed back to source.

Third quadrant: CH1 is kept off, CH_2 and CH_3 is operated. Pola
of load emf E must be reversed. With CH_3 on, load gets
connected to source V_s so both V_0, i_0 are negative leadin
to third quadrant operation. CH_3 is off, negative current free
through CH_2, D_4. V_0 and i_0 can be controlled in III quad

Fourth Quadrant:
CH_4 is operated, and other devices are kept off.
Load emf E must have its polarity reversed. With CH_4 on
positive current flows through CH_4, D_2, L and E. Inductance L
... during the time CH_4 is on. When CH4 is off, ... to load

1) For a ~~Type~~ step down chopper find the following vali... as functions of V_s, R and duty cycle α in case load is resisti...

(a) Avg. o/p voltage $V_0 = \frac{T_{on}}{T} V_s = \alpha V_s$

Avg. o/p current $I_0 = \frac{V_0}{R} = \frac{\alpha V_s}{R}$

b) Output current at the instant of commutation is V_s/R.

c) For resistive Load, f_D ~~does~~ $= 0$
RMS value of free wheeling diode current ... Zero.

(d) RMS value of o/p voltage $= \sqrt{\alpha}\, V_s$

(e) Average thyristor current $= \frac{\alpha V_s}{R}$

(f) RMS thyristor current $= \sqrt{\alpha}\, \frac{V_s}{R}$

(f) Avg. source current $= \frac{\alpha V_s}{R}$ = Avg. thyristor current

Effective i/p resistance of Chopper $= \frac{\text{DC source voltage}}{\text{average source current}}$

$$= \frac{V_s R}{\alpha V_s} = R/\alpha$$

A chopper has an input voltage of 200V, and a load of 15 ohm re... when chopper is on, its voltage drop is 1.5V and chopping frequency is ... If duty cycle is 80% find (1) Average o/p voltage (2) RMS o/p vo... (3) chopper on time.

Av. o/p voltages $= \alpha(V_s - 1.5)$

$= 0.8(200 - 1.5)$

$= 0.8 \times 198.5 = 158.8$

RMS o/p voltage $V_{or} = \sqrt{\alpha}\cdot(V_s - 1.5)$

$= 177.543$

chopper on time $- \alpha = \frac{T_{on}}{T}$

$0.8 = T_{on} \times 10 \times 10^3$

$T_{on} = 0.8$

Forced Commutation:

External elements L and C which do not carry the load current continuously are used to turn off a conducting thyristor.
Forced commutation can be achieved in two ways

(i) Voltage Commutation:

* A conducting thyristor is turned off by the reverse voltage. This reverse voltage is applied by switching a previously charged capacitor

(ii) Current Commutation:

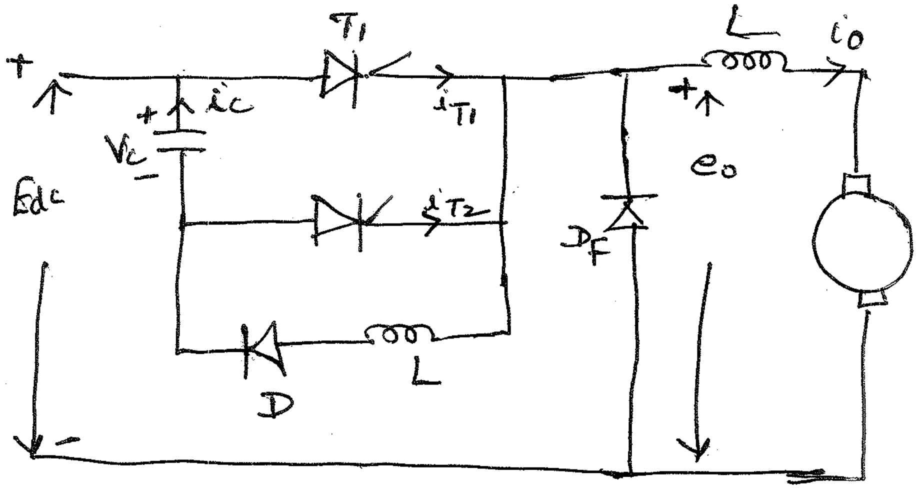
* An external pulse of current greater than load current is passed in the reversed direction through conducting SCR
* When the current pulse attains a value equal to the load current, net pulse current through thyristor becomes zero and the device is turned off.
* Current pulse is generated by initally charged capacitor

Load Commutation:

* A conducting thyristor is turned off when the load current flowing through a thyristor either
(i) becomes zero due to the nature of load circuit parameters
(ii) transferred to another device from the conducting thyristor

Voltage Commutated Chopper:

* The commutation circuit comprises an auxillary SCR T_2, a diode D, inductor L and capacitor C.
* The main power circuit comprises SCR T_1
* Initially the capacitor is charged by triggering



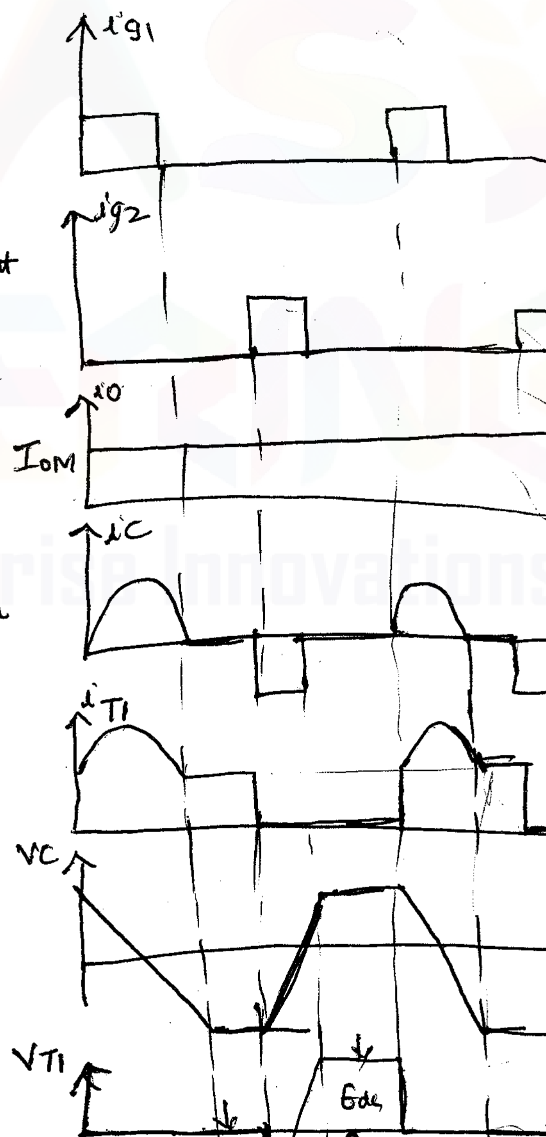
(i) Mode 1 operation:

- T_1 is triggered at t_0. Source current I_s flows in two paths, load current i_o constitutes one path and commutation current i_c, the other path
- The load voltage is equal to supply voltage $e_o = E$
- i_o flows through $E_{dc}^+ - T_1 - load - E_{dc}^-$
  Commutating current i_c through $C_+ - T_1 - L - D - C_-$
- i_c rises from zero to maximum value. when V_c becomes zero at $t = t_1/2$.
- when i_c decreases to zero, capacitor is charged to reverse voltage $(-E_{dc})$ at $t = t_1$.
- At $t = 0$, $V_{T2} = -E_{dc}$,
  $t = t_1/2$ $V_{T2} = 0$
  $t = t_1$ $V_{T2} = E_{dc}$ $I_{T_1} = I_o$, $V_c = -E_{dc}$.

Mode II operation:

- T_2 is triggered for turning off the main SCR T_1.
- Turning on of T_2 produces a reverse voltage across T_1 which turns off main SCR T_1.
- Capacitor voltage commutates the main SCR T_1, so it is called as Voltage commutated Chopper.

* T_2 provides the path for load current i_0 through $E_{dc} - C - T_2$
* load voltage is the sum of source voltage and voltage across capacitor $e_0 = E_{dc} + E_{dc} = 2E_{dc}$.
* load voltage decreases as the voltage across the capacitor decreases.
* $V_C = V_{T1}$, capacitor is directly across T_1 through T_2.
* Capacitor discharge through load, V_C and V_{T1} change from $(-E_C)$ to zero at $(t_2 + t_q)$
* e_0 from $2E_{dc}$ to E_{dc} at $(t_2 + t_q)$
* After $(t_2 + t_q)$, V_C and V_{T1} start rising from zero towards E_{dc}; e_0 starts falling to zero.

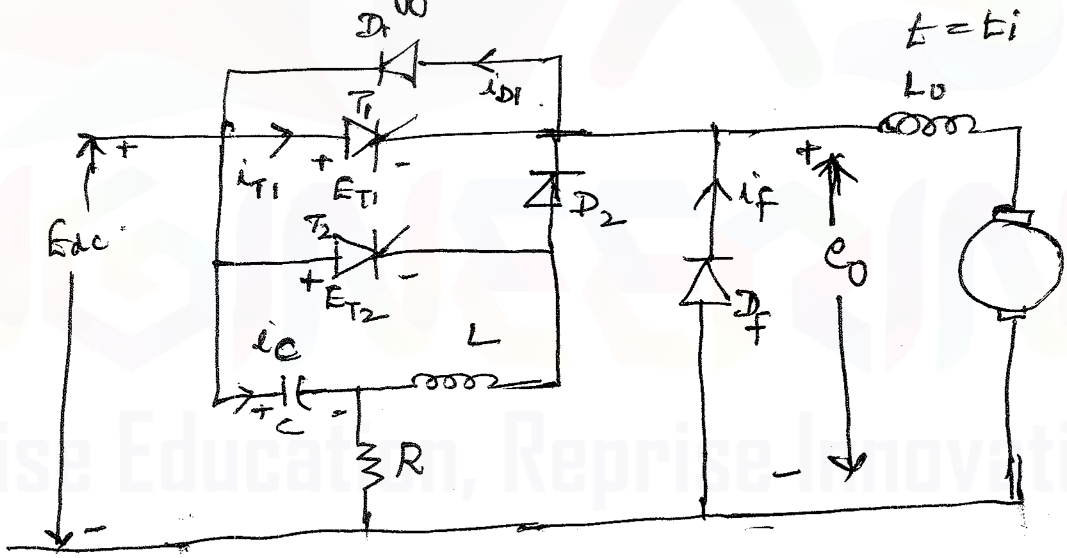


Mode III operation:- $(t_3 < t < T)$

* At t_3 $V_C = V_{T1} = E_{dc}$, $e_0 = 0$, capacitor current decays to zero, T_2 turns off naturally.
* At t_3 capacitor is slightly overcharged, freewheeling diode gets forward biased.
* Load current freewheels through diode D_F.
* During freewheeling period from t_3 to T, $V_{T2} = -ve$ when capacitor is overcharged
* $i_C = 0$, $i_{T1} = 0$, $i_f = I_{om}$, $V_{T1} = E_{dc}$, $e_0 = 0$, $i_{T2} = 0$.

Current Commutated chopper:

* T_1 is the main thyristor
* Commutation circuit consists of auxillary thyristor T_2, Ca
  inductor L, diodes D_1 and D_2.
* D_F is the freewheeling diode, R is charging resistor.
* T_1 is commutated by a current pulse generated in th
  commutation circuit.
* Reverse voltage across the device is applied through
  connected in antiparallel to the SCR.
* Energy for current commutation comes from energy st
  in a capacitor.
* Capacitor is charged to a voltage E_{dc} through
  $E_{dc}^+ - C - R - E_{dc}^-$.
* T_1 is triggered at $t=0$, so $e_0 = E_{dc}$. $\hat{I}_0 = I_{om}$
  $t = t_i$



Mode I operation:

* At time $t = t_1$, auxillary thyristor T_2 is triggered to commutate
  main thyristor T_1.
* When T_2 is turned on, oscillatory current is set up i
  the circuit consisting of C, T_2 and L.
* At t_2, the capacitor current i_c reverses, T_2 gets turne

Mode II operation:-

* T_2 is turned off at t_2, oscillatory current i_c flow through C, L, D_2 and T_1.
* at t_2, current i_c flows through thyristor T_1 and not through D
* i_c flows in opposite direction which decreases the current i_{T_1}
* At t_3, $i_c = i_{T_1}$. net current through T_1 is zero and turns off. As oscillatory current turns off, it is called as current commutated chopper.

Mode III operation:-

* T_1 is turned off at t_3,
* i_c becomes more than i_0.
* After t_3, i_c supplied load current i_0 and diode D begins to conduct the current $(i_c - i_0)$ and the drop in D_1 due to this current keeps the thyristor T_1 reverse biased for the time t_q $(t_4 - t_3)$.

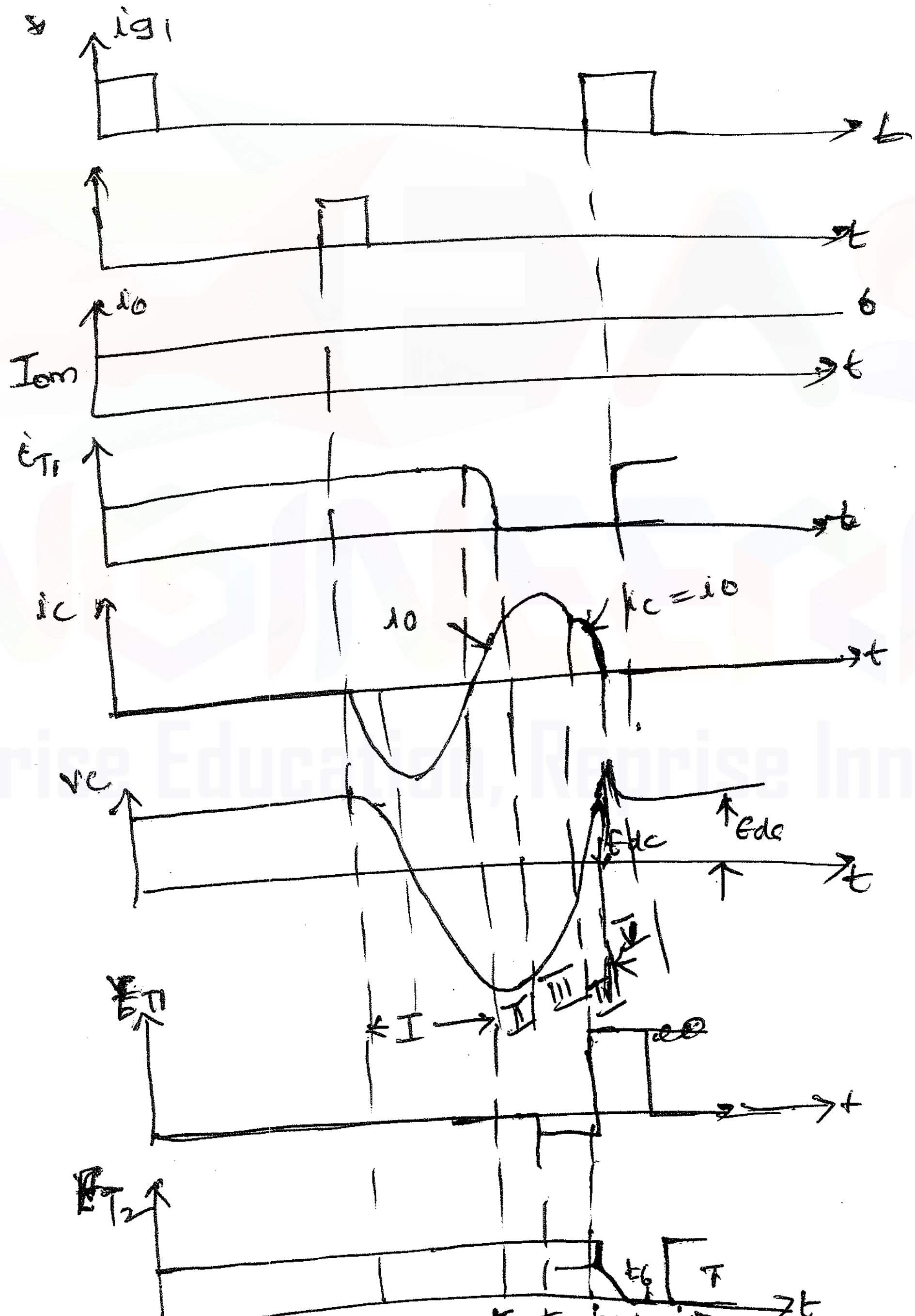
Mode IV operation:-

* At t_4 $i_c = i_0$, $i_{D_1} = 0$, D_1 is R.B.
* After t_4, a constant current equal to i_0 flows through Edc − C − L − D_2 − load. and capacitor C is charged linea to Edc at t_5. During the period $(t_4 - t_5)$ $i_c = i_0$.
* $V_c = E_{T_1}$, $e_0 = Edc - V_c$ at t_4 and t_5, $V_c = Edc$.
* At t_5 $e_0 = Edc - Edc = 0$
* V_c increase linearity and load voltage e_0 decreases t zero lineality.

Mode V operation:-

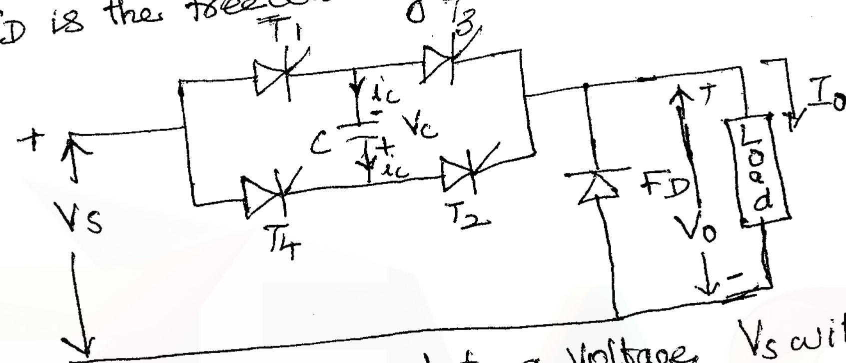
* At t_6, capacitor is overcharged to voltage greater than source voltage Edc.
* D_F becomes F.B and starts to conduct the load

* At t_6, $i_c=0$, V_c becomes more than E_{dc}.
* Interval t_5 to t_6 $i_0=i_c+i_F$, i_c decays, i_f builds up.
  At t_6, $i_f=i_0$ and $i_c=0$.
* From period t_6, load current freewheels through D_F and decays.
* As i_c is zero, D_2 is open circuited, V_c decays through R for freewheeling period of chopper.
* At $t=T$, T_1 is triggered and cycle repeats



Load Commutated Choppers

* It consist of four thyristors $T_1 - T_4$ and one commuta[ting] Capacitor C. The thyristor T_1 and T_2 acts as one pair and $T_3 T_4$ acts as second pair for conducting the load current alternately.
* T_1 and T_2 are main thyristors, T_3 and T_4, C is the comm[utating] components.
* FD is the freewheeling diode across the load.



The Capacitor is charged to a Voltage V_s with upper p[late] negative and lower plate positive.

Mode I:

* T_1 and T_2 triggered at $t = 0$, the load current flows thro[ugh] V_s, T_1, C, T_2 and load, the load voltage shoots to [...] Load current flows from source to [...] $V_0 = V_s + V_c = 2V_s$.
* Capacitor charges from V_s at $t = 0$ to $-V_s$ at t[...]
* when voltage becomes $-V_s$, the load voltage falls from $2V_s$ to 0 at $t = t_1$.
* At $t = 0$, T_1 and T_2 are turned on, $T_3 T_4$ reverse bias[ed] by capacitor Voltage
* At $t = t_1$, T_1 and T_2 are turned off, $T_3 T_4$ forward bi[ased]

Mode II:

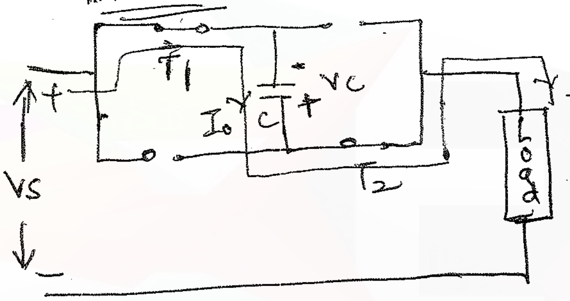
* At t_1, Capacitor slightly overcharged, Freewheeling diode gets forward biased and load current transferre[d] from T_1, T_2 to FD.

$V_0 = \ldots \; V_c = 0, \; i_c = 0, \; i_{fd} = I_0$

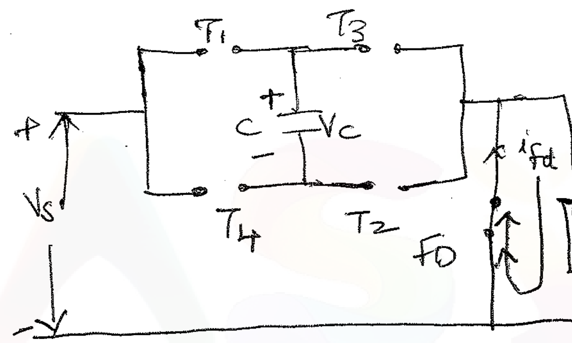
Mode - III

* At t_2, T_3 T_4 is triggered, load voltage at once becomes $V_0 = V_s + V_c = 2V_s$.
* T_1 and T_2 are reverse biased, and turned off at t_2
* Load current flows through V_s, T_4, C, T_3 and load charges capacitor linearly from $(-V_s)$ at t_2 to V_s at
* Load voltage falls from $2V_s$ at t_2 to zero at t
* During $(t_3 - t_2)$; $i_c = -I_0$, $V_{T_1} = V_{T_2} = -V_s$ at t_2 and V_s at t_3.

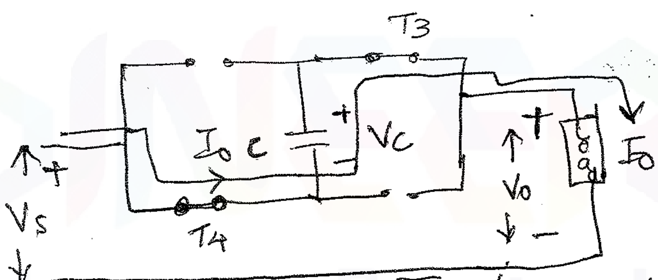
Mode 1



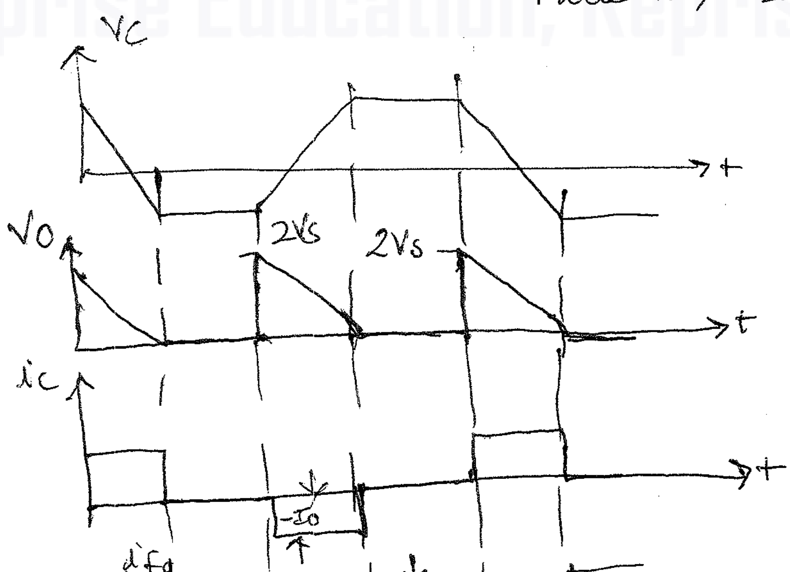
$0 < t < t_1$



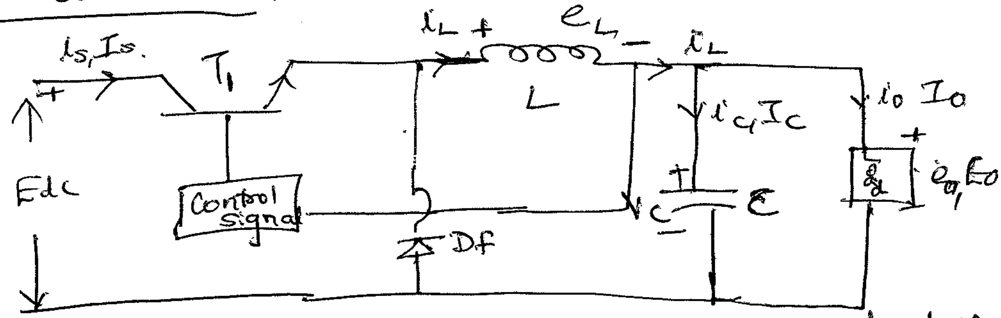
Mode-II $t_1 < t < t_2$



Mode III, $t_2 < t < t_3$.



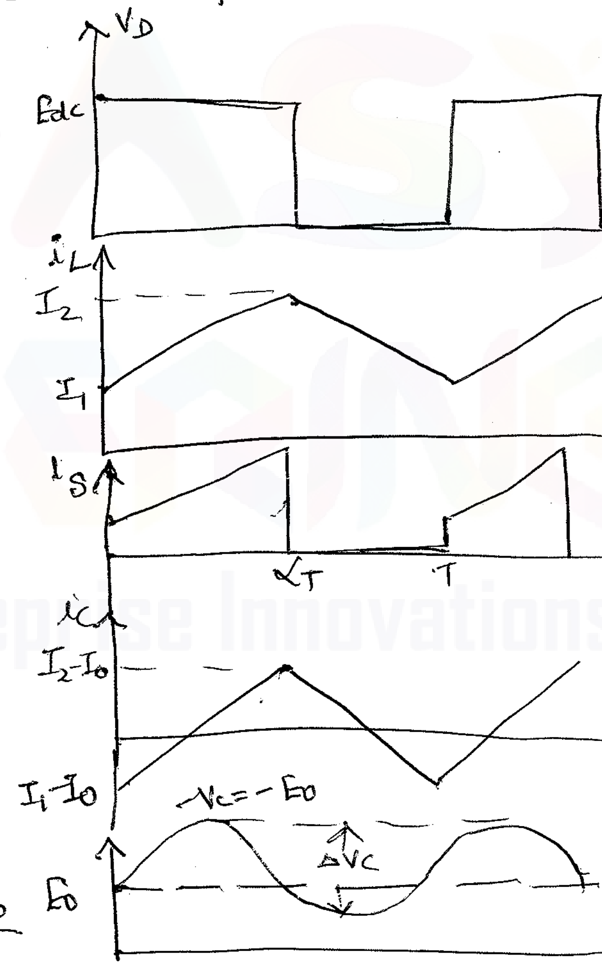
Buck Converter:



The converter produce a lower average output voltage E_o tha[n]
the dc input voltage Edc. By varying T_{on}/T the average
output voltage can be controlled. Transistor T_1 is switched
on at time $t=0$. The supply current flows through filter
inductor, filter capacitor and load resistor R_L. The inductor st[ores]
energy during the Ton period. During the interval when trans[istor]
is on, diode is reverse biased and the input provides energ[y]
to the load as well as to the inductor. Now at instant $t=T_{on}$
transistor T_1 is switched off. During the interval when transist[or]
is off, inductor current flows through L, C load and
freewheeling diode Df and hence diode Df conducts.

Voltage across inductor L

$$e_L = L\frac{di}{dt}$$



During time Ton, the inductor current rises linearly from I_1 to I_2

$$E_{dc} - E_o = L\left(\frac{I_2 - I_1}{T_{on}}\right)$$

$$E_{dc} - E_o = \frac{\Delta I L}{T_{on}}$$

$$T_{on} = \frac{\Delta I \cdot L}{E_{dc} - E_o}$$

During Toff i_L falls from I_2 to I_1

$$-E_o = -L\frac{\Delta I}{T_{off}}$$

$$T_{off} = \frac{\Delta I \cdot L}{E_o}$$

$$\Delta I = \frac{E_{dc} - E_o}{L} T_{on} = \frac{T_{off} E_o}{L}$$

$$E_{dc} T_{on} - E_o T_{on} = T_{off} E_o$$

$$E_o T_{off} + E_o T_{on} = E_{dc} T_{on}$$

$$E_o (T_{off} + T_{on}) = E_{dc} T_{on}$$

$$E_o \cdot T = E_{dc} T_{on}$$

$$E_o = \frac{E_{dc} \cdot T_{on}}{T} \; ; \; E_o = \alpha E_{dc}$$

$$\alpha = \frac{T_{on}}{T}$$

$$E_{dc} I_s = E_0 I_0 = \alpha E_{dc} I_0$$
$$I_s = \alpha I_0$$

$$T = T_{on} + T_{off}$$

$$T = \frac{\Delta I L}{E_{dc} - E_0} + \frac{\Delta I L}{E_0}$$

$$T = \frac{1}{f} = \frac{\Delta I L E_{dc}}{E_0 (E_{dc} - E_0)} \qquad \Delta I = \frac{E_0 (E_{dc} - E_0)}{L E_{dc}} \cdot T$$

$$\Delta I = \frac{E_0 (E_{dc} - E_0)}{f \cdot L \cdot E_{dc}}$$

$$\Delta I = \frac{E_0 (E_{dc}/E_{dc} - E_0/E_{dc})}{f \cdot L \cdot E_{dc}/E_{dc}}$$

$$\alpha = \frac{E_0}{E_{dc}} \qquad \Delta I = \frac{\alpha E_{dc} (1-\alpha)}{f \cdot L}$$

$$i_L = i_c + i_0$$

When load ripple current ΔI_0 is very small then Δ

The average capacitor current which flows for $T_{on}/2 + T_{off}/$

$$I_c = \frac{\Delta I}{4}$$

Capacitor voltage is expressed as

$$V_c = \frac{1}{C} \int i_c \, dt + V_c(t=0)$$

Peak to peak ripple voltage of capacitor is

$$\Delta V_c = V_c - V_c(t=0)$$
$$= \frac{1}{C} \int_0^{t/2} \frac{\Delta I}{4} \, dt$$
$$= \frac{\Delta I \cdot T}{8C} = \frac{\Delta I}{8fc}.$$

$$\Delta V_c = \frac{E_0 (E_{dc} - E_0)}{8 L C f^2 E_{dc}}$$

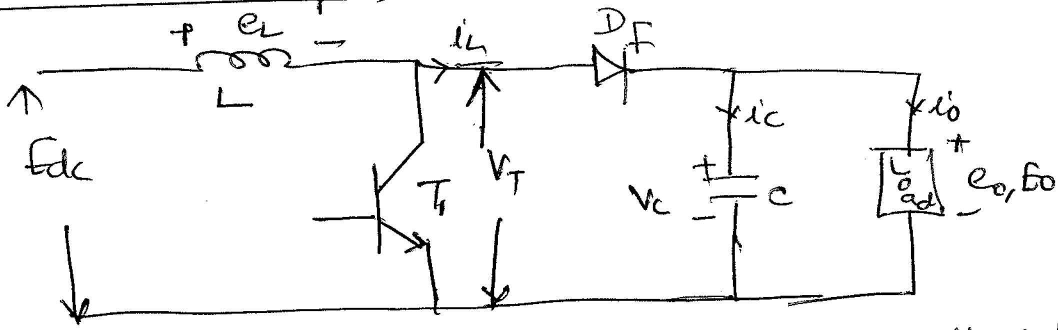
$$\boxed{\Delta V_c = \frac{E_{dc} \, \alpha (1-\alpha)}{8 L C f^2}}$$

The main application is in regulated dc power supplies
dc motor speed control.

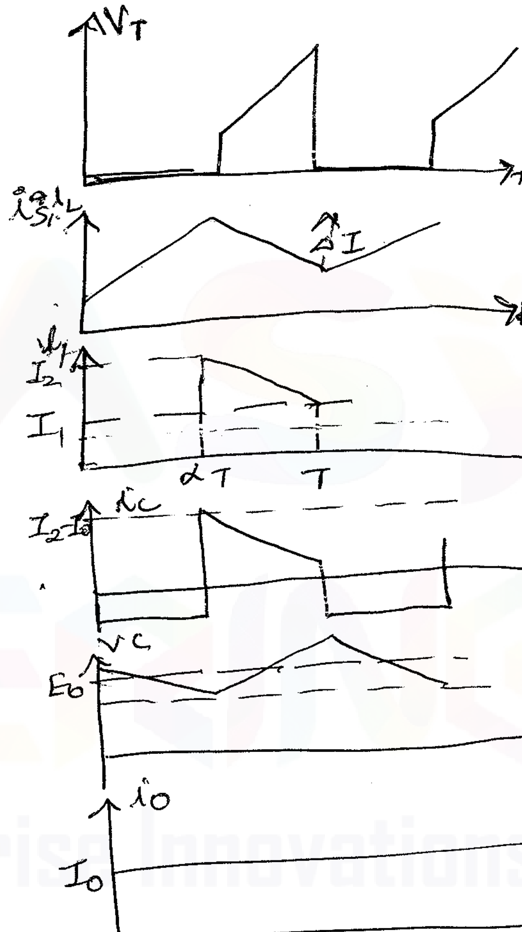
Disadvantage:

1. The i/p current is discontinuous.
2. Input filter is required for smoothing purpose
3. It gives one polarity of output voltage and unidi
output current.
... circuit needed for diode D_f be

Boost converter (step up):



The output voltage is always greater than i/p voltage. The inductor stores energy during on period Ton. Diode D_F is reverse biased and isolates the output stage. when the power transistor is off, the o/p stage receives energy from the inductor as well as from the input. The current which was flowing through the transistor would now flow through L, D_F, C and load.



During Ton

$$E_{dc} = L\left(\frac{I_2 - I_1}{T_{on}}\right) = L\frac{\Delta I}{T_{on}}$$

$$T_{on} = \frac{\Delta I L}{E_{dc}}$$

During Toff

$$E_{dc} - E_o = -L\frac{\Delta I}{T_{off}}$$

$$T_{off} = \frac{\Delta I L}{E_o - E_{dc}}$$

$$\Delta I = \frac{E_{dc} T_{on}}{L} = \frac{(E_o - E_{dc}) T_{off}}{L}$$

$$E_o = E_{dc}\frac{T}{T_{off}}$$

$$E_o = \frac{E_{dc}}{1-\alpha}$$

Assuming a loseless circuit $P_i = P_o$

$$E_{dc} I_s = E_o I_o = \frac{E_{dc} I_o}{(1-\alpha)}$$

Average i/p current $I_s = \frac{I_o}{1-\alpha}$

$$T = \frac{1}{f} = T_{on} + T_{off}$$

$$= \frac{\Delta I L}{E_{dc}} + \frac{\Delta I L}{E_o - E_{dc}}$$

$$T = \frac{\Delta I L E_o}{E_{dc}(E_o - E_{dc})}$$

Peak ripple current

$$\Delta I = \frac{E_{dc}(E_o - E_{dc})}{f L E_o}$$

$$\Delta I = \frac{E_{dc}\alpha}{fL}$$

$$\Delta V_c = V_c - V_c(t=0)$$

$$\Delta V_c = \frac{1}{C}\int_0^{T_{on}} I_c dt = \frac{1}{C}\int_0^{T_{on}} I_o d$$

$$\Delta V_c = \frac{I_o T_{on}}{C}$$

$$T_{on} = \frac{E_o - E_{dc}}{E_{dc}} T_{off}$$

$$E_{dc} = \frac{E_o T_{off}}{T} = E_o T_{off} \cdot f$$

$$T_{on} = \frac{(E_o - E_{dc})}{E_o T_{off} \cdot f} T_{off} = \frac{E_o - E_{dc}}{E_o \cdot f}$$

Applications

1. Regulated dc power supplies
2. Regenerative braking of dc motors

Advantages:

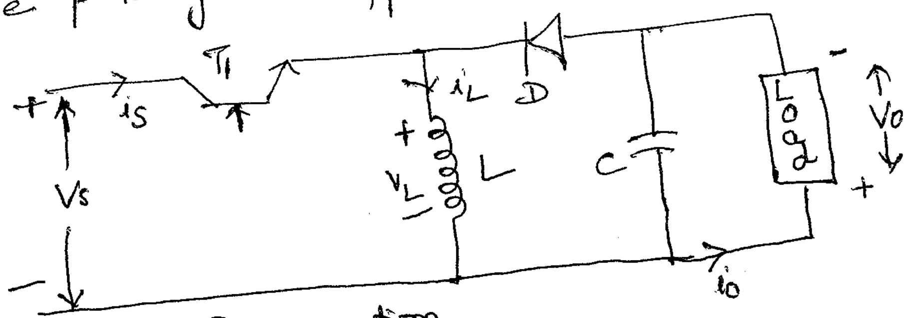
1. Regulator steps up the voltag
2. High efficieny
3. Input current is continuous.

Disadvantages:

1. High peak current flows through transistor T_1.
2. Areeage o/p voltage is very sensitive to cha in duty cycle α.
3. Circuit needs larger filter capacitor and larger because of higher rms current flow through & C.

Buck Boost Regulator:

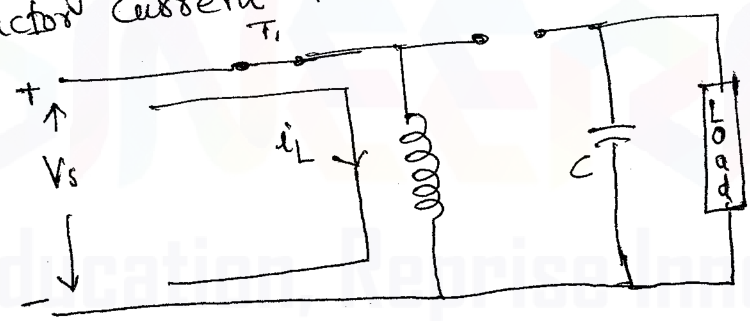
A buck boost regulator provides an output voltage greater or less than i/p voltage. This is also called inverting regulator since the output voltage polarity is opposite to that of the supply volt



Two modes of operation

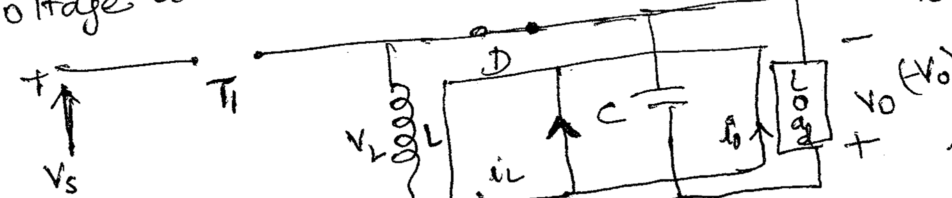
Mode I:

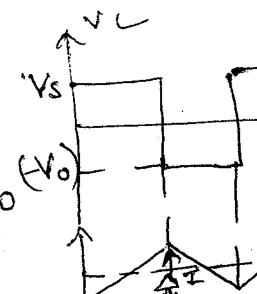
* Transistor T_1 turned on by the base signal
* At $t=0$, T_1 comes to ON state and diode D is reverse biased
* I_s flows through T_1 and inductor L.,
* During the on period inductor stores energy and inductor current increases from I_1 to I_2.



Mode II

* At $t=t_1$, Transistor T_1 is switched off.
* Current flows through inductor L, capacitor C, and Diode D and also to load. Forward biased.
* Inductor current decreases from I_2 to I_1.
* Voltage across the inductor is $-V_o$.





Analysis:

Inductor current increases from I_1 to I_2 in on th period

$$V_S = L\frac{I_2 - I_1}{T_{on}} = L\frac{\Delta I}{T_{on}}$$

$$T_{on} = \frac{\Delta I L}{V_S}$$

$$\Delta I = \frac{V_S T_{on}}{L} \quad \text{--- (1)}$$

Inductor current decreases from I_2 to I_1 in the off period of chop

$$V_0 = -L\frac{\Delta I}{T_{off}} \qquad T_{off} = -\frac{\Delta I L}{V_0} \qquad \Delta I = -\frac{T_{off} V_0}{L}$$

Comparing eq (1) & (2)

$$\Delta I = \frac{V_s T_{on}}{L} = -\frac{T_{off} V_0}{L}$$

$$V_s T_{on} = -T_{off} V_0 \qquad V_0 = -\frac{V_s T_{on}}{T_{off}} = \frac{-V_s T_{on}}{T - T_{on}} = \frac{-V_s \alpha}{1-\alpha}$$

$$\alpha\text{-duty cycle} = \frac{T_{on}}{T}$$

Output voltage $V_0 = \frac{-V_s \alpha}{1-\alpha} = -\frac{V_s T_{on} f}{1 - T_{on} f}$

$$V_0 (1 - T_{on} f) = -V_s T_{on} f$$

$$V_0 - V_0 T_{on} f = -V_s T_{on} f \Rightarrow -V_0 T_{on} f + V_s T_{on} f = V_0$$

$$T_{on} (V_0 - V_s) f = V_0$$

$$T_{on} = \frac{V_0}{(V_0 - V_s) f}$$

Assume no loss in circuit

$$V_s I_s = -V_0 I_0 = \frac{\alpha V_s I_0}{1-\alpha}$$

$$\boxed{I_s = \frac{I_0 \alpha}{1-\alpha}}$$

Switching period $T = T_{on} + T_{off}$

$$= \frac{\Delta I L}{V_s} + \frac{\Delta I L}{V_0}$$

$$T = \Delta I L \frac{(V_0 - V_s)}{V_s V_0}$$

$$\Delta I = \frac{V_s V_0}{f L (V_0 - V_s)}$$

$$\boxed{\Delta I = \frac{V_s \alpha}{f L}}$$

When Transistor is on, Capacitor Supplies the load current

$$\Delta V_c = \frac{1}{C}\int_0^{T_{on}} I_c\, dt = \frac{I_0 T_{on}}{C}$$

Sub $T_{on} = \frac{V_0}{(V_0 - V_s) f}$

$$\boxed{\Delta V_c = \frac{I_0 V_0}{(V_0 - V_s) f C}}$$

$$\Delta V_c = \frac{I_0 \alpha}{f C}$$

Resonant Converter

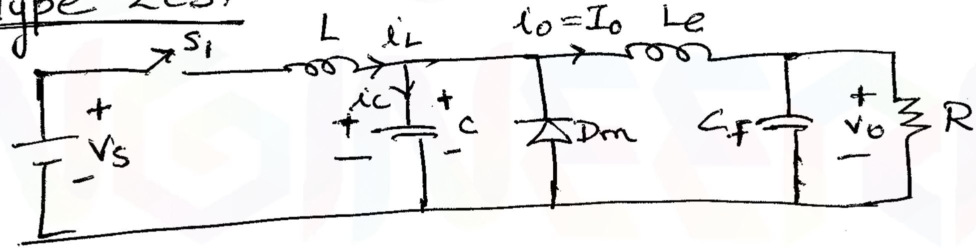
The switches are made to turn on and turn off at the entire load current at high di/dt. The devices having high di/dt experience high voltage stress across them. because of this high power losses in switching devices. If size and weight of components are increased, switching frequencies are increased. Another drawback is high di/dt and dv/dt causes electromagnetic interference.

These problems can be minimised ~~by~~ when each switch can be turned on and off when the voltage across it or current through it is zero at the instant of switching. The converter which employ zero voltage and zero current are called Resonant Converters.

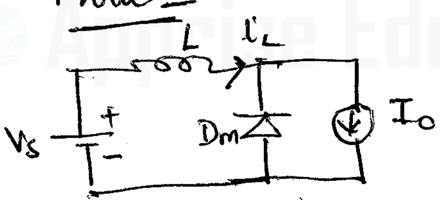
Zero Current Switching Resonant converters

When the switch current is zero, there is a current $i = C_j \frac{dv}{dt}$ flowing through the internal capacitance C_j due to finite slope of the switch voltage at turn off.

L-Type ZCS:



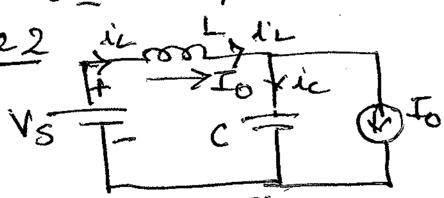
Mode I



S_1 is turned on and diode D_m conducts. $i_L = \frac{V_s}{L} t$

$0 \le t \le t_1$

Mode 2



S_1 on, D_m is off

$i_L = I_m \sin\omega_0 t + I_0$

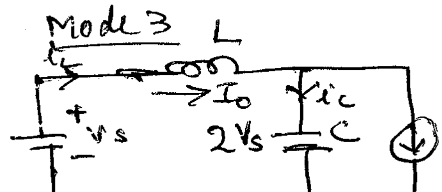
$= i_c + I_0$

$V_c = V_s(1 - \cos\omega_0 t)$

$V_{c(pk)} = 2V_s$ since $t_2 = \frac{\pi}{2}\sqrt{LC}$

$V_{c2} = 2V_s$ $t_2 = \pi\sqrt{LC}$

Mode 3



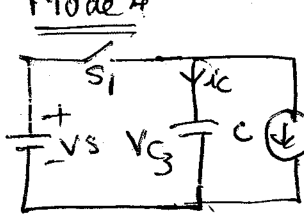
$i_L = I_0 - I_m \sin\omega_0 t$

$V_c = 2V_s \cos\omega_0 t$

$i_L = 0$ at $t = t_3$

$V_c(t = t_3) = V_{c3}$.

Mode 4



$V_c = V_{c3} - \frac{I_0}{C} t$

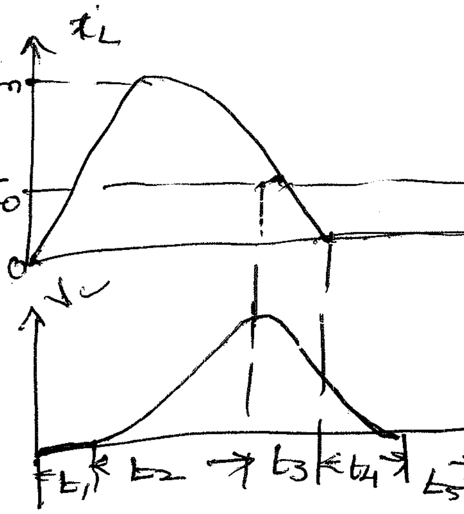
$t_4 = \frac{V_{c3} C}{I_0}$

Mode 5 $(0 \le t \le t_5)$

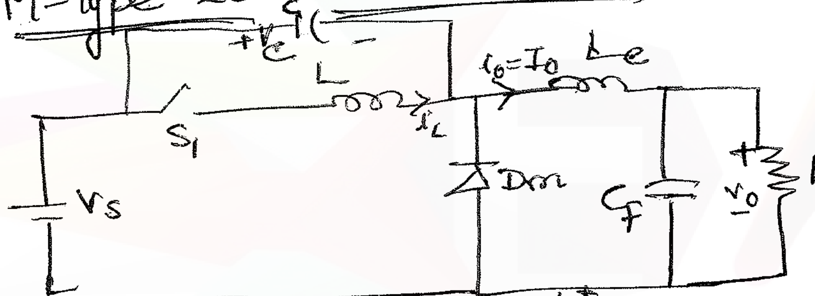
When capacitor voltage tends to be negative diode D_m ... Load current I_0 flows through the diode D_m.

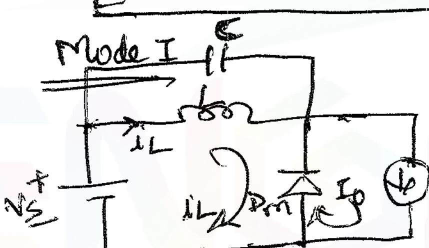
$t_5 = T - (t_1 + t_2 + t_3 + t_4)$.

The peak switch voltage equals $I_0 + I_m$ the supply voltage V_s. Since the switch current is zero at turn off and turn on, the switching loss becomes very small. The peak resonant current must be greater than the load current I_0. This sets a limit on the minimum value of load resistance R. By placing an antiparallel diode across the switch, the o/p voltage can be insensitive to load variations.

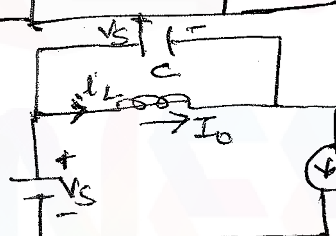


M-Type ZCS Resonant Converters

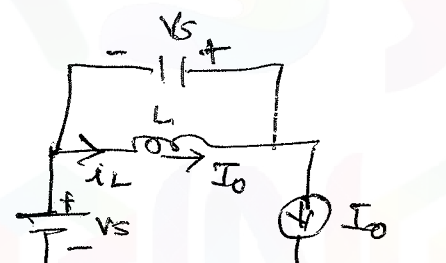




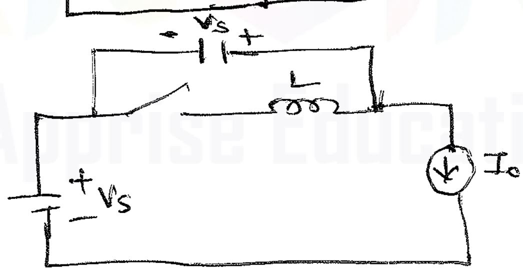
Mode I



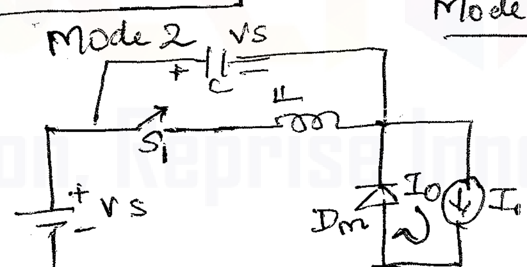
Mode 2



Mode 3



Mode 4



Mode 5

Mode 1: $i_L = \frac{V_s}{L} t$

D_m conducts. $t_1 = I_0 L / V_s$

Mode 2

$V_c = V_s \cos \omega_0 t$

$V_{C(PK)} = V_s$ at end of t_2

$V_c(t = t_2) = V_s$

Mode 3

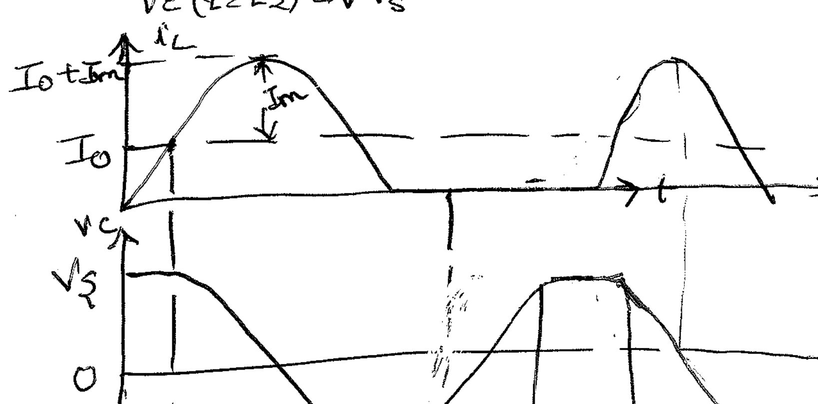
$V_c = -V_s \cos \omega_0 t$

$V_c(t = t_3) = V_{c3}$

Mode 4:

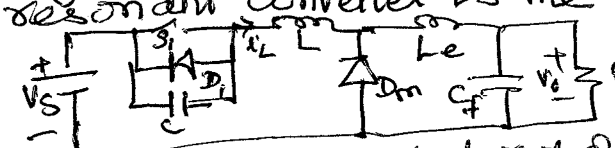
$t = t_4$, $V_c(t = t_4) = V_s$

$t_4 = (V_s - V_{c3}) C / I_0$



Zero Voltage Switching Resonant Converters :-

The switches are turned off and turn on at Zero voltage. The Capacitor C is connected in parallel with the switch S_1 to achieve ZVS. If diode is Connect in series with S_1 the Voltage across C can oscillate freely and switch is operated in a full wave Configuration. ZVS resonant Converter is the dual of ZCS resonant Converter.



Mode 1

S_1 and diode Dm are off, Capacitor C charges at a Constant rate of load current $V_c = \frac{I_o t}{C}$. $V_c(t=t_1) = V_s$ $t_1 = V_s C / I_o$

Mode 2 : $0 \le t \le t_2$.

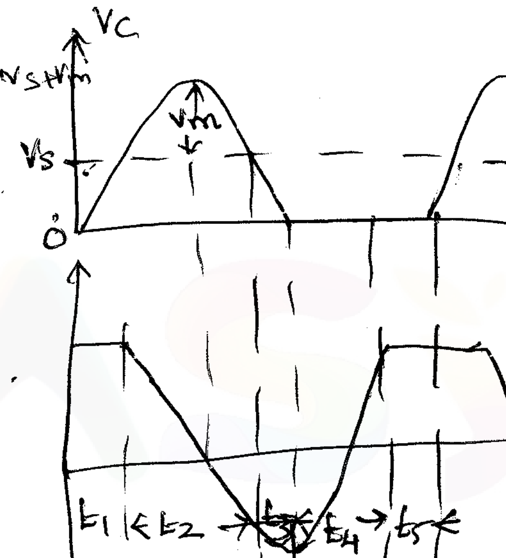
S_1 is still off, but diode Dm turns off.

$V_c = V_m \sin\omega_0 t + V_s$ $V_m = I_o \sqrt{L/C}$

$V_{T(PK)} = V_{C(PK)} = I_o \sqrt{\frac{L}{C}} + V_s$

The inductor current $i_L = I_o \cos\omega_0 t$.

$V_c(t=t_2) = V_s$ $i_L(t=t_2) = -I_o$.



Mode 3 :- $0 \le t \le t_3$.

$V_c = V_s - V_m \sin\omega_0 t$

$V_c = V_s - V_m \sin\omega_0 t$ $i_L = -I_o \cos\omega_0 t$.

$t_3 = \sqrt{LC}\,\sin^{-1} x$. $x = V_s / V_m$

Mode 4

S_1 is turned on, diode Dm remains on,

$i_L = I_{L3} + \frac{V_s}{L} t$.

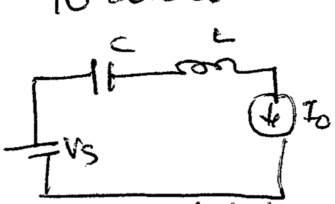
$t_4 = (I_o - I_{L3})(L/V_s)$.

Mode 5 : $0 \le t \le t_5$.

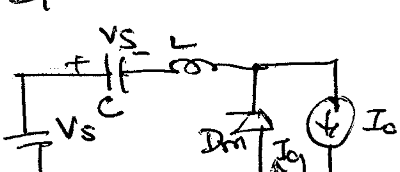
S_1 is on but Dm is off. Load current I_o flows through the switch. This mode ends at time $t = t_5$.

$t_5 = T - (t_1 + t_2 + t_3 + t_4)$.

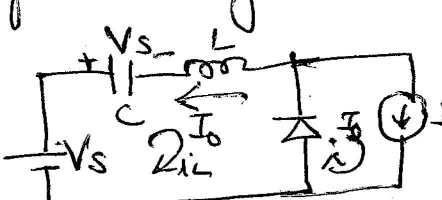
ZVS converter are used for constant load application. The peak switch voltage dependent on load current I_o. S_1 must be turned on at Zero Voltage otherwise energy will be dissipated. To avoid this D_1 must conduct before turning on the switch.



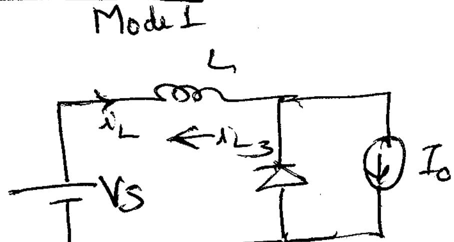
Mode 1



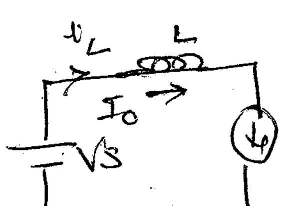
Mode 2



Mode 3



Mode 4



Mode 5.

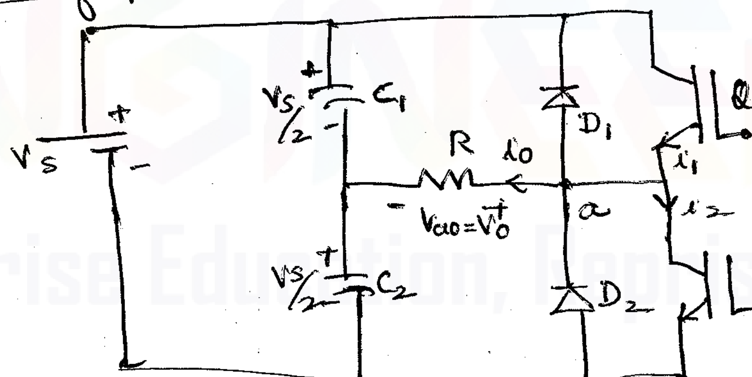
Inverters

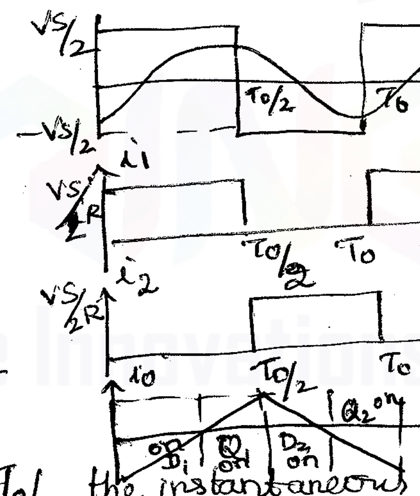
Dc to ac Converters are known as inverters. The function of inverter is to change a dc i/p voltage to symmetric ac o/p voltage of desired magnitude and frequency. The o/p voltage could be fixed or variable at a fixed or variable frequency. The o/p voltage of ideal inverter should be Sinusoidal. For low and medium power applications, square wave or quasi sq wave voltage but for high power applications, low distorted Sinusoidal waveforms are required. The harmonic Content of o/p voltage can be minimized or reduced significantly by switching techniques.

Inverters are used in industrial applications like variable sp ac motor drives, induction heating, standby power supplies, and uninterruptible power supplies.

Inverters are Classified into two types (1) single phase inv and (2) three phase inverters. Each type can use controlle turn on and turn off devices. The inverters generally use PWM control signals for producing an ac o/p voltage. An inverter is calle ~~i/p vo~~ voltage fed inverter (VFI) if the i/p voltage remains constant Current fed inverter (CFI) if the i/p current is maintained constant A variable dc linked inverter if the i/p voltage is controllable.

Principle of operation:





when one transistor Q_1 is turned on for a time $T_0/2$ the instantaneous voltage across the load V_0 is $V_s/2$. If transistor Q_2 is only turned on a time $T_0/2$, $-V_s/2$ appears across the load. Q_1 and Q_2 are not turned on at the same time. The inverter requires a three wire dc source and when a transistor is off, its reverse voltage is V_s, instead of $V_s/2$. This inverter is known as a half bridge Inverter

rms o/p Voltage $V_0 = \left[\frac{2}{T_0}\int_0^{T_0/2} \frac{V_s^2}{4} dt\right]^{1/2} = V_s/2.$

For inductive load the load current cannot change immediately if Q_1 is turned off at $t = T_0/2$; the load current would continue to f through D_2, load and lower half of dc source until the current fal

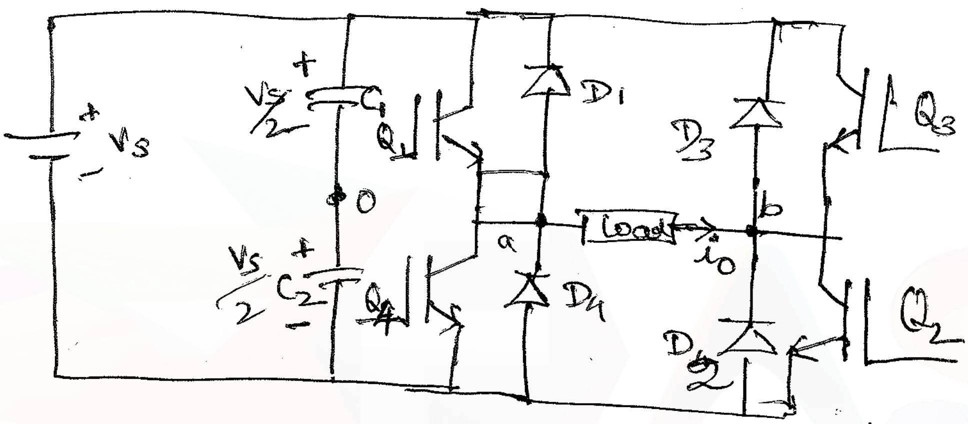
When diode D_1 or D_2 conducts, energy is fedback to dc source and these diodes are known as feedback diodes.

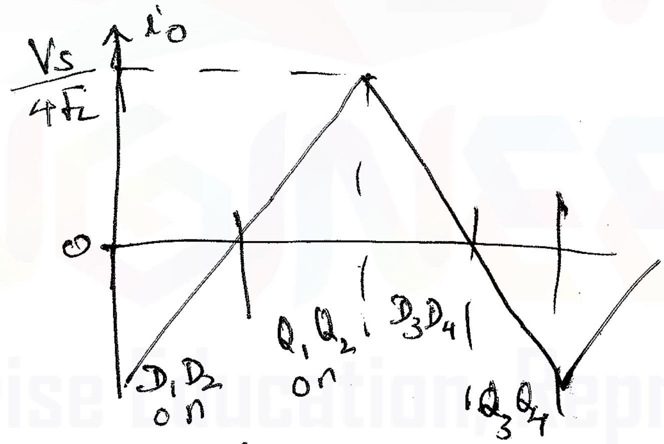
Single phase bridge Inverter

A single phase voltage source inverter is shown. It consists of four choppers. When Q_1 and Q_2 are turned on the i/p voltage V_s appears across the load. If Q_3 and Q_4 are turned on, the voltage across the load is reversed and is $-V_s$.

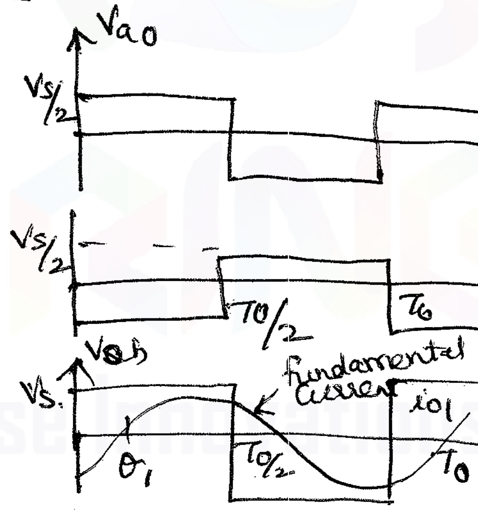
The rms o/p voltage

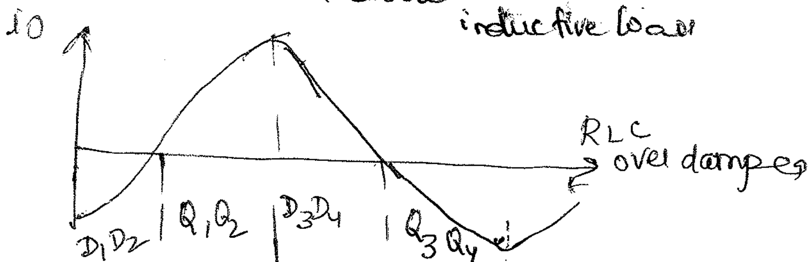
$$V_o = \left[\frac{2}{T_o}\int_0^{T_o/2} V_s^2 \, d\theta\right]^{1/2} = V_s$$

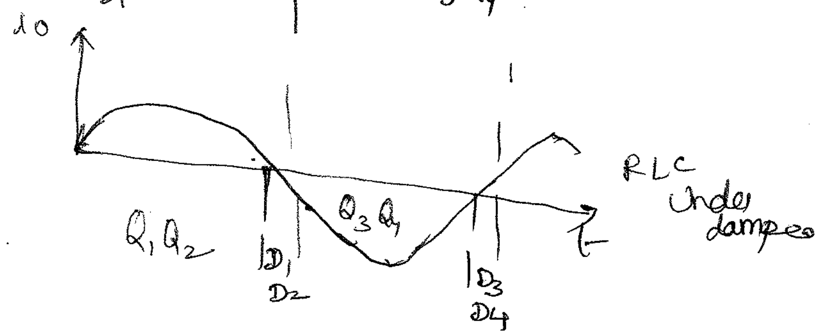




Load current with inductive load

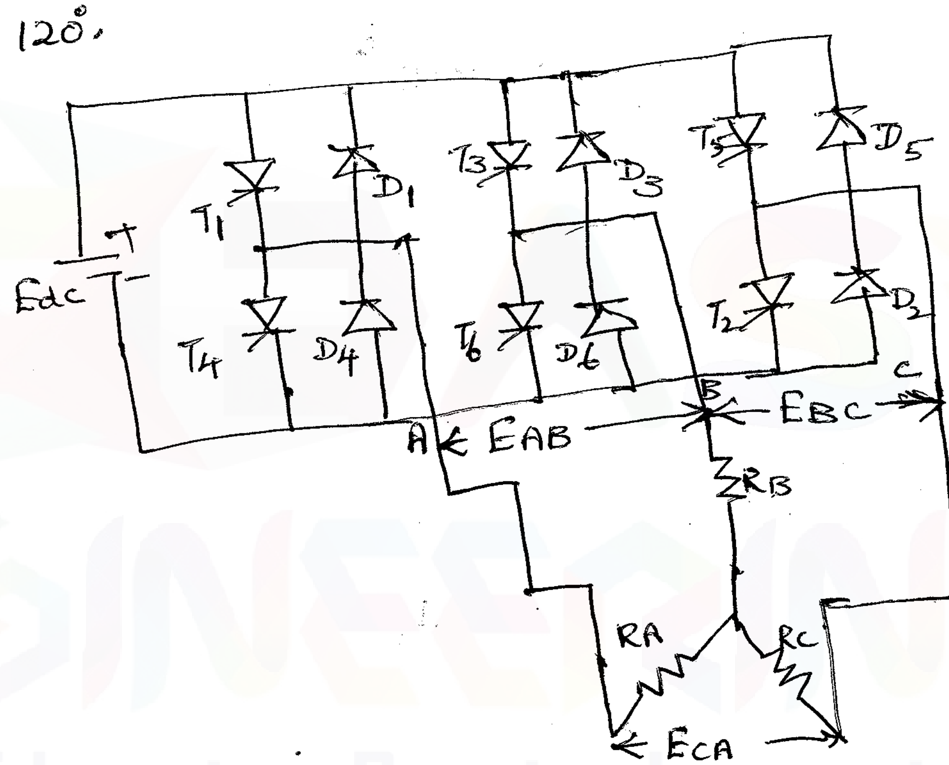






Three phase Bridge Inverters

In applications such as UPS and ac motor drives, three-phase inverters are used. It is possible to supply a three-phase load by means of three seperate single phase inverters, where each inverter produces an o/p displaced by 120° with respect to each other. The inverter is termed as six step bridge inverter. In inverter a step is defined as a change in the firing from one thyristor to next thyristor in proper sequence. For a cycle of 360°, each step would be of interval for a six step inverter. There are two possible scheme of gating the thyristors. In one scheme each thyristor conducts for 180°, In other scheme each thyristor conducts for 120°.



180° conduction mode

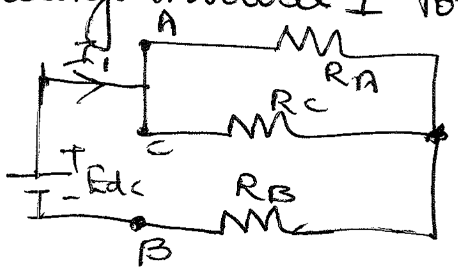
A maximum of three thyristors conduct at any instant and each SCR conducts for π radians in every cycle of the o/p. Thyristor pair in each leg, (ie) T_1, T_4; $T_3 T_6$; and $T_5 T_2$ are turned on with a time interval of 180°. Each SCR T_1 conducts for 180° and SCR T_4 for next 180° of a cycle. Thyristors in the upper group (ie) T_1, T_3, T_5 conduct at an interval of 120°. If SCR T_1 is fired at 0°, T_3 must be triggered at 120° and T_5 at 240°. Same is true for lower group of thyristors.

$T_1 T_6 T_5$ – I interval, $T_1 T_6 T_2$ → II interval, $T_1 T_3 T_2$ – III,
$T_4 T_3 T_2$ – IV interval, $T_4 T_3 T_5$, – V interval, $T_4 T_6 T_5$ – VI

... of 60° duration, only three SCRs are conducting

For a star connected load, the line to neutral volt
must be ~~form~~ determined to find line or phase cu

(i) During interval I for $0 \le \omega t \le \pi/3$. $(T_1\, T_6\, T_5)$

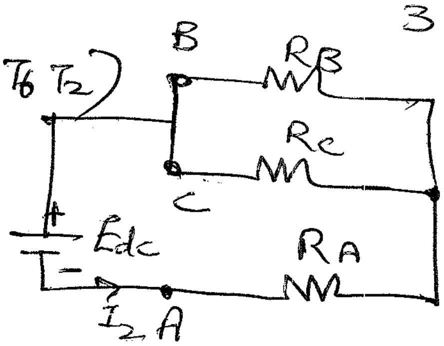


$$R_{eq} = R_B + (R_A \| R_C)$$
$$= R + R/2 = 3R/2 \quad (R_A = R_B$$
$$I_1 = \frac{E_{dc}}{R_{eq}} = \frac{2E_{dc}}{3R}$$

$$E_{AN} = E_{CN} = \frac{I_1 R}{2} = \frac{E_{dc}}{3} \qquad E_{BN} = -I_1 R = -\frac{2E_{dc}}{3}$$

(ii) II interval $\pi/3 \le \omega t < 2\pi/3$ $(T_1\, T_6\, T_2)$

$$R_{eq} = R + R/2 = 3R/2$$
$$I_2 = \frac{E_{dc}}{R_{eq}} = \frac{2E_{dc}}{3R}$$
$$E_{AN} = I_2 R = \frac{2E_{dc}}{3}$$
$$E_{BN} = E_{CN} = -\frac{I_2 R}{2} = -\frac{E_{dc}}{3}$$



(iii) III interval $2\pi/3 \le \omega t < \pi$

$$R_{eq} = R + R/2 = 3R/2$$
$$I_3 = \frac{E_{dc}}{R_{eq}} = \frac{2E_{dc}}{3R}.$$
$$E_{AN} = E_{BN} = \frac{I_3 R}{2} = \frac{E_{dc}}{3} \qquad E_{CN} = -I_3 R = -\frac{2E_{dc}}{3}.$$

Line voltage $E_{AB} = E_{AN} - E_{BN}$; $E_{BC} = E_{BN} - E_{CN}$; $E_{CA} = E_{CN}$

The phase voltages have six steps per cycle and line v
have one positive pulse and negative pulse per cycle
The instantaneous line to line voltage E_{AB}

$$E_{AB} = \sum_{n=1,3,5}^{\infty} \frac{4E_{dc}}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t + \pi/6).$$

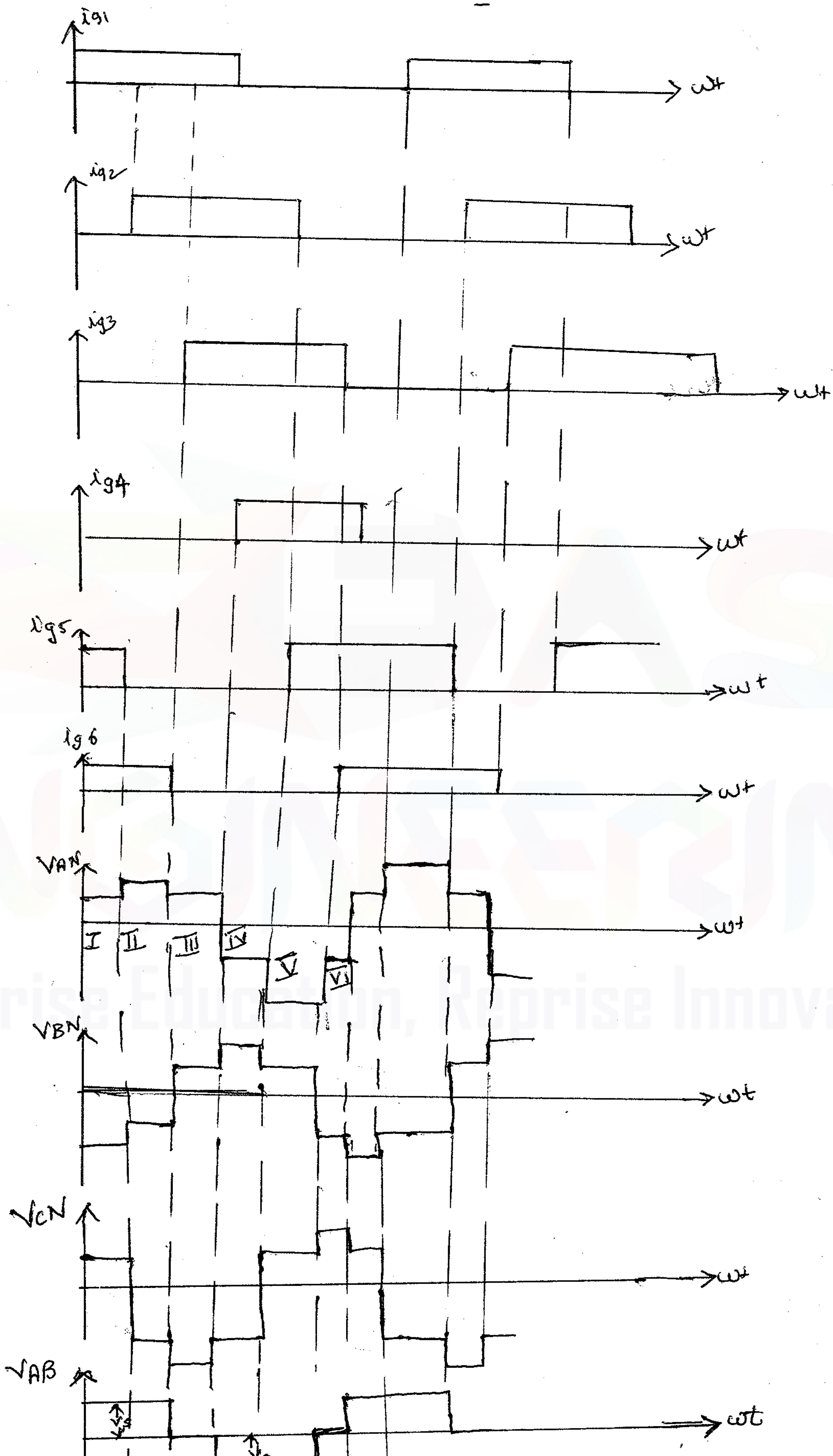
$$E_{BC} = \sum_{n=1,3,5}^{\infty} \frac{4E_{dc}}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t - \pi/2)$$

$$E_{CA} = \sum_{n=1,3,5}^{\infty} \frac{4E_{dc}}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t - 7\pi/6)$$

$n = 3, 9, 15 \ldots$ $\cos\frac{n\pi}{6} = 0$

Line to line RMS voltage $E_L = \left[\frac{2}{\pi}\int_0^{2\pi/3} E_{dc}^2\, d(\omega t)\right]^{1/2} = \sqrt{\frac{2}{3}}\, E_{dc}$

Three phase 180° Conduction mode



Comparison of two Conduction modes:

* In 180°, when I_{g1} is removed to turn off SCR T_1 at ωt = gating signal I_{g4} is Simultaneously applied to turn on SC T_4 in Same leg.
* Commutation interval must exist between the rem of I_{g1} and application of I_{g4} for proper and reliable operation
  * This problem can be avoided by 120° mode of Conduc
* In this 60° interval between turning off T_1 and turning on of T_4.
* SCR T_1 can be commutated safely.
* No short circuit occurs between the same leg, and one terminals remains open for all characte
* So 180° is preferred in three phase inverters.

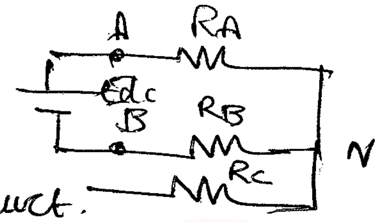
Three phase 120° Conduction mode :-

Each thyristor conducts for 120°. At any instant, only two thyristor remain on. Like in the above case each thyristor conducts for 120°. The firing sequence are given below.

I interval	– $T_1\ T_6$
II "	– $T_1\ T_2$
III "	– $T_3\ T_2$
IV	– $T_3\ T_4$
V	– $T_5\ T_4$
VI	– $T_5\ T_6$

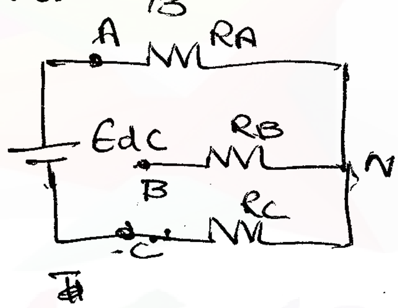
Each thyristor conduct at a time, one from upper group and other from lower group.

(i) I Interval, $0 < \omega t < \pi/3$ $T_1 T_6$ Conduct.



$E_{AN} = \frac{E_{dc}}{2}$ $E_{BN} = -\frac{E_{dc}}{2}$ $E_{CN} = 0$

(ii) II interval $\pi/3 \le \omega t \le 2\pi/3$. $T_1 T_2$ Conduct.



$E_{AN} = \frac{E_{dc}}{2}$ $E_{BN} = 0$

$E_{CN} = -E_{dc}/2$

(iii) III interval $2\pi/3 \le \omega t \le 3\pi/3$. $T_2\ T_3$ conduct

$E_{AN} = 0$, $E_{BN} = \frac{E_{dc}}{2}$ $E_{CN} = -E_{dc}/2$.

The line to neutral voltage

$$E_{AN} = \sum_{n=1,3,5}^{\infty} \frac{2E_{dc}}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t + \pi/6)$$

$$E_{BN} = \sum_{n=1,3,5}^{\infty} \frac{2E_{dc}}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t - \pi/2)$$

$$E_{CN} = \sum_{n=1,3,5}^{\infty} \frac{2E_{dc}}{n\pi} \cos n\pi/6 \sin n(\omega t - 7\pi/6)$$

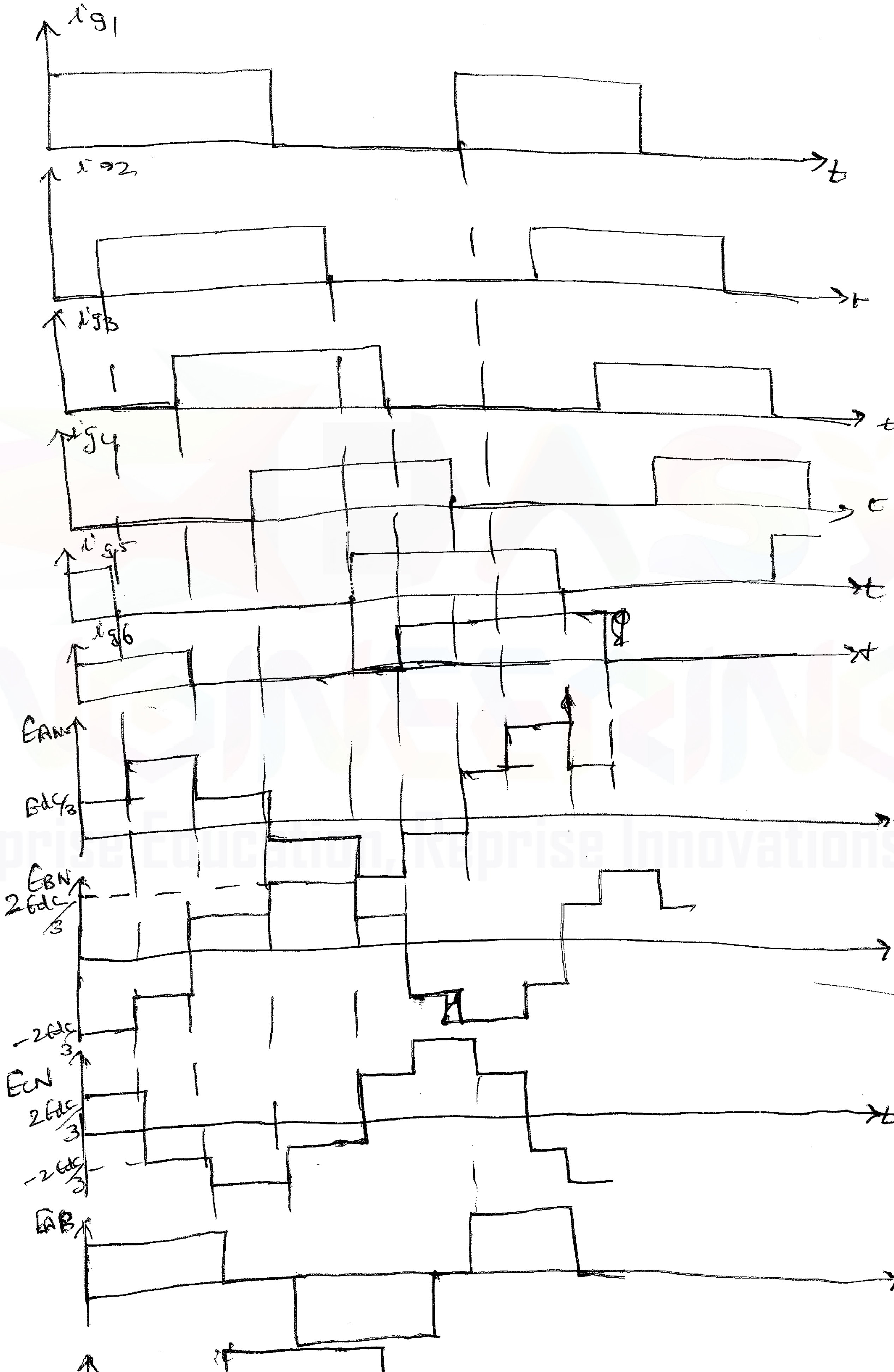
There is a delay of $\pi/6$ between the turning of T_1 and turning of T_4.

$$E_{Ln} = \frac{4 E_{dc}}{\sqrt{2}\, n\pi} \cos n\pi/6 \qquad E_{L1} = \frac{4 E_{dc} \cos 30}{\sqrt{2}\, \pi}$$

$$E_{L1} = 0.7797 E_{dc}$$

RMS value of line to neutral voltage

$$E_p = \frac{E_L}{\sqrt{3}} = \frac{\sqrt{2}\, E_{dc}}{3}$$



Voltage Control of Inverters:

The output voltage of inverter may not remain constant due to the variations in the input voltage and voltage drop in inverter. The methods used are

a) External control of ac output voltage
b) External control of dc input voltage
c) Internal control of Inverter.

External control of Ac output voltage:

* Ac voltage controller is inserted between the out[put] terminals of inverter and load terminals. By controlling t[he] ac voltage controller using the firing angle, the voltage i[nput] to ac load is regulated
* This method produces higher harmonic content in output voltage, when the output voltage from the ac voltage controller is at low level.

External Control of DC Input Voltage

* The dc input voltage to the inverter is controlled through a fully controlled rectifier, uncontrolled rectifier and chopper, or through an ac voltage controller and an uncontrolled rectifier.
* In case the available voltage is dc, then dc inpu[t] voltage is controlled by chopper.

Advantages of Voltage control schemes

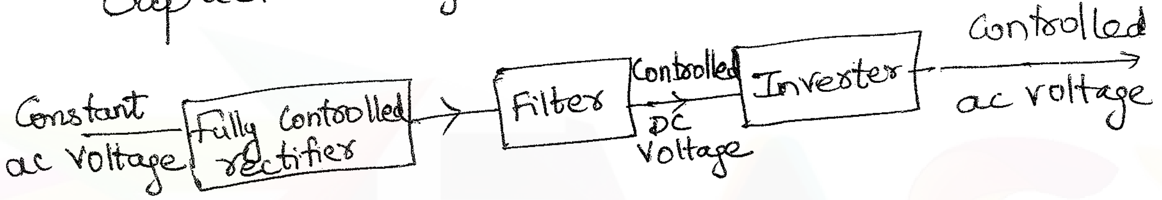
1. The output voltage waveform and harmonic content not affected as the inverter output voltage is controlled.

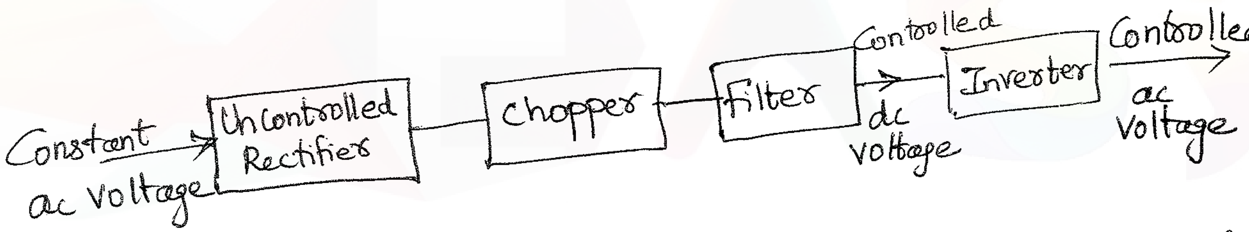
... Voltage Control scheme

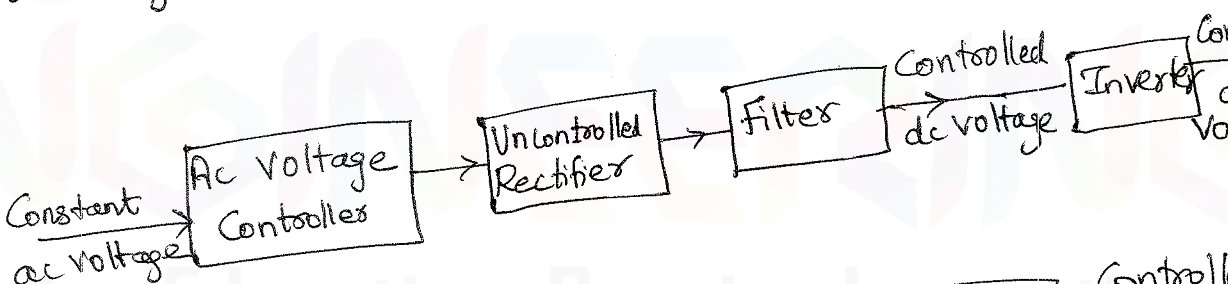
1. Number of power converters varies from two to three.
Hence more losses and reduces efficiency of entire sc

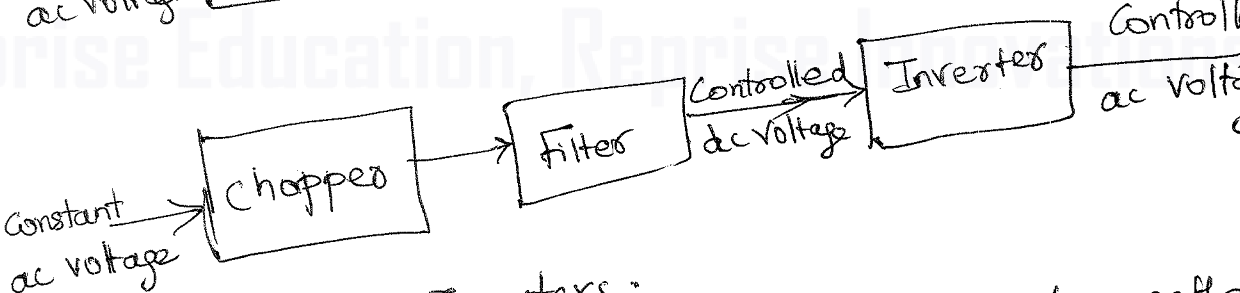
2. For reducing the ripple content of dc voltage inpu
to inverter, filter circuit is required which increas
the cost, weight and size and at the same time
reduces efficiency and makes the transient respon
sluggish.

3. As the dc input is decreased, the commutating
capacitor voltage decreases.





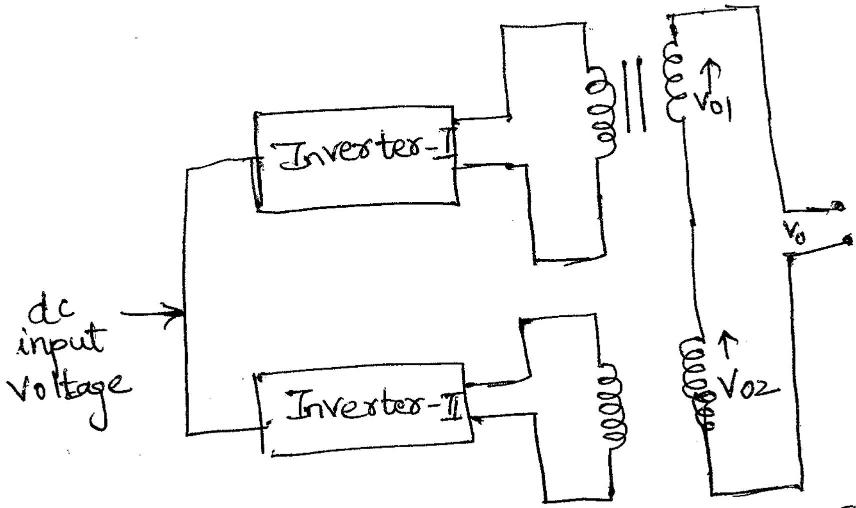


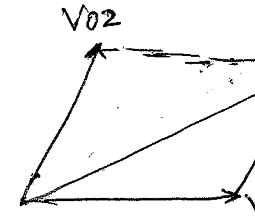


Internal Control of Inverters :-

Inverter can be controlled Internally by two metho
(i) Series Inverter control (ii) Pulse width Modulatio
Control.

1. Series Inverter Control:-





The output voltage of two inverters can be summ
up with the help of transformers to obtain an adjustable
output voltage. The inverter output is fed to two transfo
whose secondaries are connected in series.

$$V_0 = \left[V_{01}^2 + V_{02}^2 + 2V_{01}V_{02}\cos\theta\right]^{1/2}$$

The frequency of V_{01}, V_{02} from two inverters is sam

$\theta = 0$, $V_0 = V_{01} + V_{02}$,

$\theta = \pi$ $V_0 = 0$ in case $V_{01} = V_{02}$

The series connection of inverter is called mult
converter control.

Pulse width Modulated Inverters:-

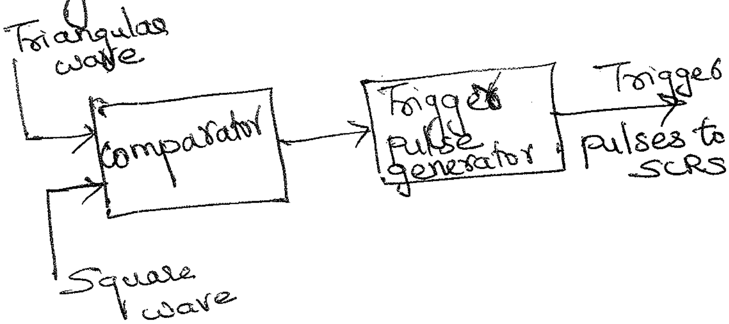
The width of the pulses are modulated to ob
inverter output voltage control and to reduce its harm
content. Different PWM techniques are
(a) Single pulse modulation (b) Multiple pulse mod
(c) Sinusoidal PWM (d) Modified Sinusoidal PWM.

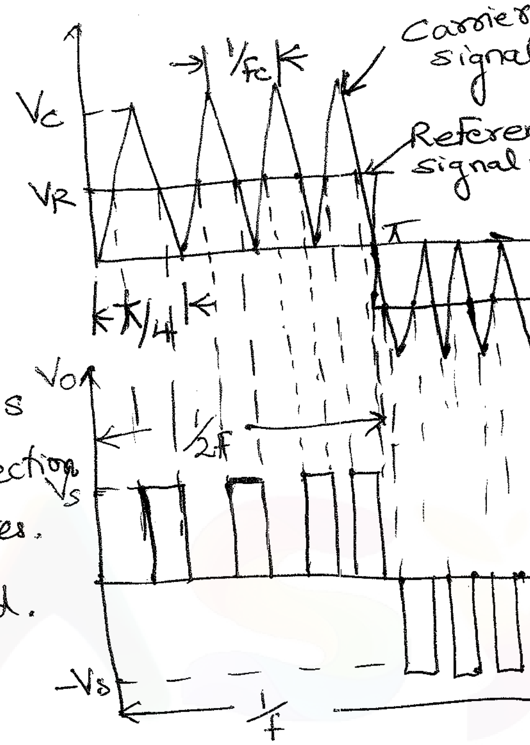
Multiple pulse Modulation:-

Several equal pulse per half cycle are obtaine
... reference signal with a triangular carrier
... for turning on

and turning off IGBT.

The Carrier frequency determines the number of pulses per half cycle m, whereas the frequency of reference signal sets the output frequency fo.





The triggering pulses for thyristors are generated based on the intersection of Carrier and reference signal waves. When $V_c > V_r$ pulses are generated.

Carrier frequency fc determines the number of pulse per half cycle.

Modulation frequency is the ratio of Carrier frequency to reference frequency

$$m_f = \frac{f_c}{F_o}$$

The number of pulses per half cycle. $N_p = \frac{f_c}{2f_o} = \frac{m_f}{2}$.

Variation of Modulation varies from 0 to 1,
Pulse width varies from 0 to π/N_p.
Output voltage from 0 to V_s.

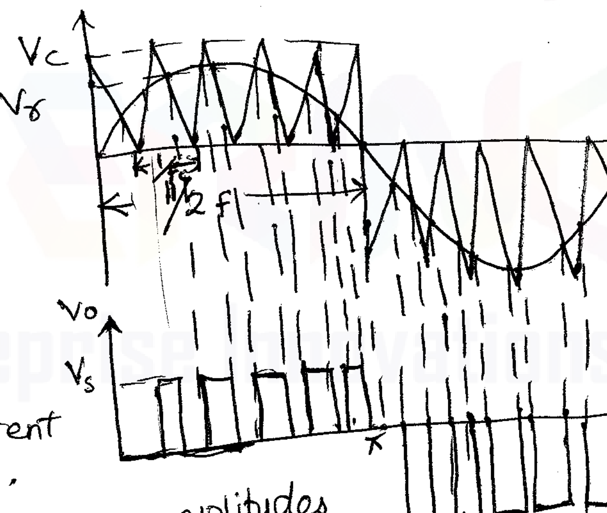
The rms output voltage $V_{L(rms)} = \left[\frac{2N_p}{2\pi} \int_{(\pi/N_p - P)/2}^{(\pi/N_p + P)/2} V_s^2 \, d(\omega t) \right]^{1/2}$

$$V_{L(rms)} = V_s \sqrt{\frac{N_p \cdot P}{\pi}}$$

Sinusoidal pulse width Modulation:-

* Several pulses per half cycle are used as in the case of Multiple pulse modulation. The width is equal for all pulses. In case of sinusoidal pulse modulation, pulse width is a Sinusoidal function of angular position of the pulse in a cycle

* A high frequency carrier wave V_c is compared with a sinusoidal reference wave V_r of the desired frequency.
* The intersection of V_c and V_r determines the switching instants and commutation of the modulated pulse.
* V_c is the peak value of triangular carrier wave. V_r is the reference or modulating signal.
* When modulating signal is higher than triangular signal the pulses will be generated.



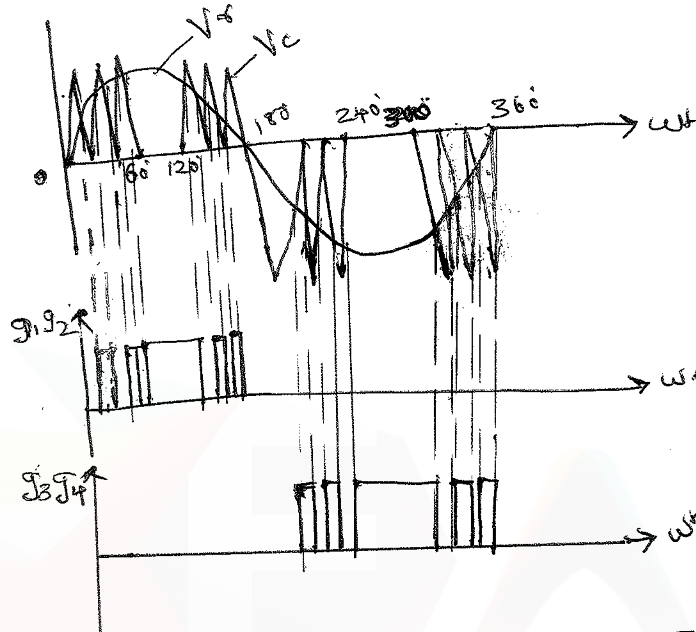
* There are N pulses per half cycle. When triangular carrier wave has its peak coincident with zero of reference signal.
* The ratio of V_r/V_c is called modulation index and it controls the harmonic content of o/p voltage waveform.

(i) For MI < 1, largest harmonic amplitudes in the o/p voltage are associated with harmonics of order $f_c/f+1$, or 2N+1. By increasing the number of pulses, order of dominant harmonic frequency can be raised which can be filtered easily.

(ii) For MI > 1, lower order harmonics appear, since pulse ... a sinusoidal function of angular

Modified Sinusoidal pulse width Modulation:-

Sine and Triangular wave are compared to genera[te] the pulse. Triangular is the carrier signal which is applied for first and last 60° per half cycle. (0 to 60° and 120° to 18[0°]



when $V_r > V_c$ pulses are generated. The output pulses are fed to inverter.

Advantages:

* Fundamental Component is increased
* Harmonics characteristics are improved
* Reduces the number switching of power semiconductor devices
* Switching losses are reduced.

Reduction of Harmonics in the inverter output voltage:-

* The output voltage of inverter may have harmonic co[ntent] much higher than 5% of its fundamental Component.
* Filters are connected between the load and invert[er to] bring the harmonic content to a reasonable l[evel]
* For high frequency harmonics, low size filters [are] used, for low frequency harmonics, filter size incr[eases] which makes the circuit bulky, costly and weight[y]

Harmonic Reduction by — Single PWM

The width of the pulse is adjusted to reduce the harmonic. The RMS value of the amplitude of harmonic voltage of a single pulse modulated wave is given by

$$V_{Ln} = \frac{4V_{dc}}{\sqrt{2}n\pi} \sin\frac{np}{2}$$

$$= \frac{2\sqrt{2}V_{dc}}{n\pi} \sin\frac{np}{2}$$

P is width of pulse, To reduce third order harmonic, $V_{L3} = 0$

$$V_{L3} = \frac{2\sqrt{2}V_{dc}}{3\pi} \sin\frac{3P}{2} = 0$$

$$\sin\frac{3P}{2} = 0$$

$$P = 120^\circ$$

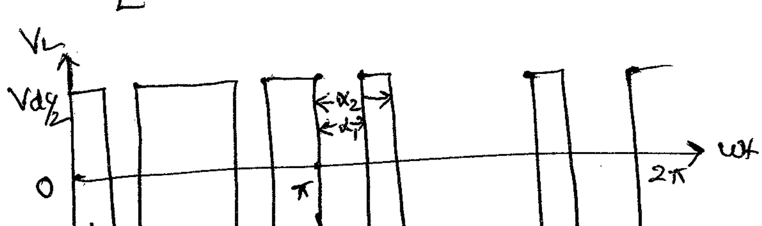
Ill^ly to Eliminate 5^{th} harmonic $P = 72^\circ$

Harmonic Reduction by Multiple Commutation in Each Half cycle

Instead of having commutation at the end of half cycle, some more commutations can be created in the half cycle. By selecting proper values of α_1 and α_2 lower order harmonics can be eliminated. The amplitude of voltage wave Vdc. Multiple commutation employs four commutation per cycle instead of one. For unmodulated square wave, the voltage waveform has quarter wave symmetry. $B_n = 0$

$$A_n = \frac{4V_{dc}}{\pi 2}\left[\int_0^{\alpha_1} \sin n\omega t\,(d\omega t) - \int_{\alpha_1}^{\alpha_2} \sin n\omega t\,(d\omega t) + \int_{\alpha_2}^{\pi/2} \sin n\omega t\, d\omega t\right]$$

$$= \frac{2V_{dc}}{\pi}\left[\frac{1 - 2\cos n\alpha_1 + 2\cos n\alpha_2}{n}\right]$$



Third and fifth harmonics are eliminated then

$$A_3 = \frac{2E_{dc}}{\pi}\left[1 - \frac{2\cos 3\alpha_1 + 2\cos 3\alpha_2}{3}\right] = 0$$

$$A_5 = \frac{2E_{dc}}{\pi}\left[1 - \frac{2\cos 5\alpha_1 + 2\cos 5\alpha_2}{5}\right] = 0$$

$$1 - 2\cos 3\alpha_1 + 2\cos 3\alpha_2 = 0 \quad \text{— (1)}$$

$$1 - 2\cos 5\alpha_1 + 2\cos 5\alpha_2 = 0 \quad \text{— (2)}$$

The two equation are solved to obtain

$\alpha_1 = 23.62°$ and $\alpha_2 = 33.6°$

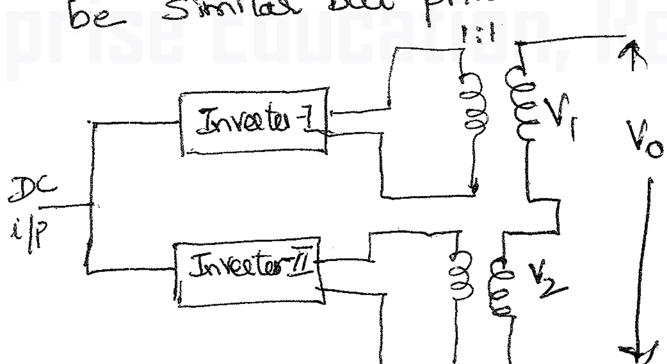
IIIly any two harmonics can be eliminated by calculating the corresponding values of α_1 and α_2. This method produces a fundamental voltage of 83.9% or 0.839 times the amplitude fundamental component of unmodulated voltage wave. The inverter is derated by (100 − 83.9) 16%.

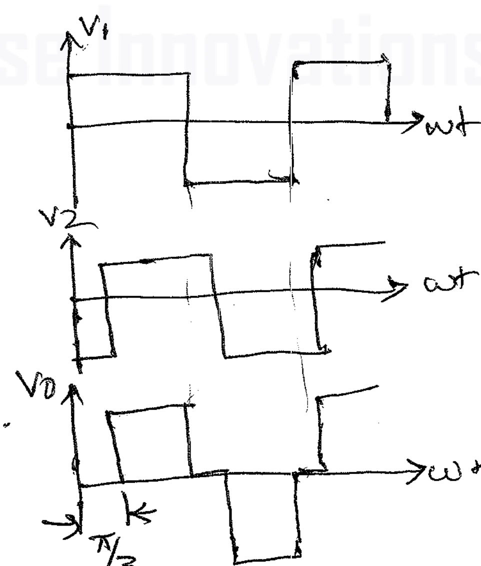
Disadvantages:

Four commutations per cycle which leads to more switching losses and decreases the efficiency of operation.

Harmonic Reduction by Transformer Connection:

* The output voltage from two or more inverters can be combined by means of transformers.
* The output waveforms from the inverters must be similar but phase shifted from each other.





* The waveform V_2 has a phase shift of $\pi/3$ with respect to V_1.
* By adding V_1 and V_2 the resultant output voltage V_o is obtained.

$V_o = A_1 \sin\omega t + A_3 \sin 3\omega t + A_5 \sin 5\omega t$

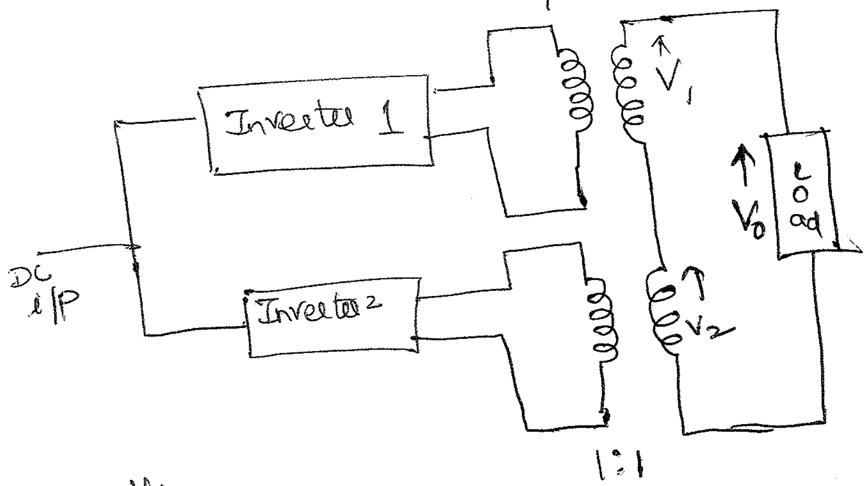
* The phase shifting of $\pi/3$ and combining voltages by transformer connection eliminate third order haemonics.
* Along with third haemonics multiple of 3rd, 9th, 12th are eliminated
* The resultant fundamental component is not twice the individual voltage but it is $\sqrt{3}/2$ times the individual o/p voltage the effect is reduced by $(1-\sqrt{3}/2) = 13.4$

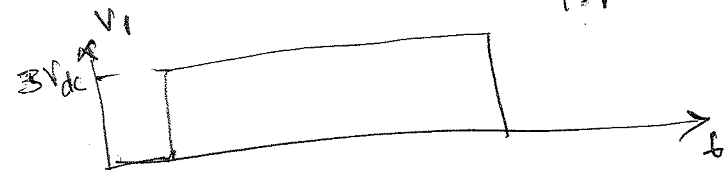
Disadvantage

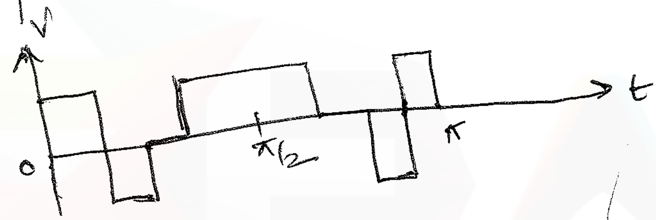
* More number of inverters and transformers of same r

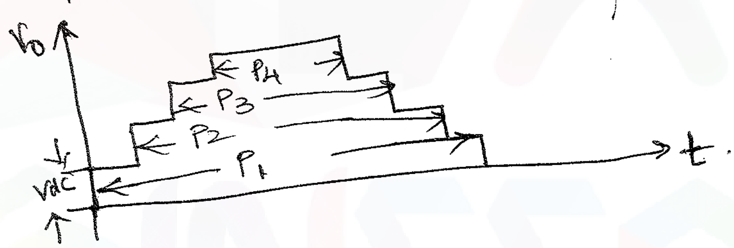
Harmonic Reduction by Stepped wave Inverters.

* The pulses of different widths and heights are added to produce a resultant stepped wave with reduced haemonic content.
* The inverters are connected to a common load thro transformers having turns ratio 1:3 and 1:1 respective
* Inverter 1 produced an output voltage V_1. The output may be zero or positive during first half cycle.
* During negative cycle the output may be zero or negative.
* This type of output is called two level modula
* Inverter 2 produces an output voltage V_2. The outp may be positive, zero and negative during the first half cycle. So it is called three level modula
* The resultant output voltage is a combination of Inverter 1 and Inverter 2.
* The amplitude of output voltage is 4Vdc and the wave form has four steps.
* The amplitude depends on the value of P_1, P_2, P_3, P_4 and amplitude of Vo.
* By selecting proper parameter, 3rd, 5th & 7th can be reduced considerably.


Inverter 1
Inverter 2
DC
i/P
V1
V2
V0
load
1:1


V1
3Vdc
t


V
0
t
π/2
π


V0
P4
P3
P2
P1
Vdc
t

Space Vector Pulse width Modulation (SVPWM)

* SVPWM is a digital modulation technique where the objective is to generate PWM load line voltage that are in average equal to a given load line voltages.
* SVPWM generates a reference voltage vector (V_{REF}) whose angular speed calculate the desired value of synchronous speed of the motor and its magnitude determines the required voltage(V_s) that will maintain a constant air gap f
* The concept of space vector is derived from rotating field of AC machine which is used for modulating the inverter output voltage.
* The three phase quantities can be transformed to their equivalent 2 phase quantity either in synchronously rotating frame (or) stationary frame.
* From the 2 phase reference vector magnitude can be obtained and used for modulating the inverter output

$$V_a = V_m \sin\omega t$$

$$V_b = V_m \sin(\omega t - 2\pi/3)$$

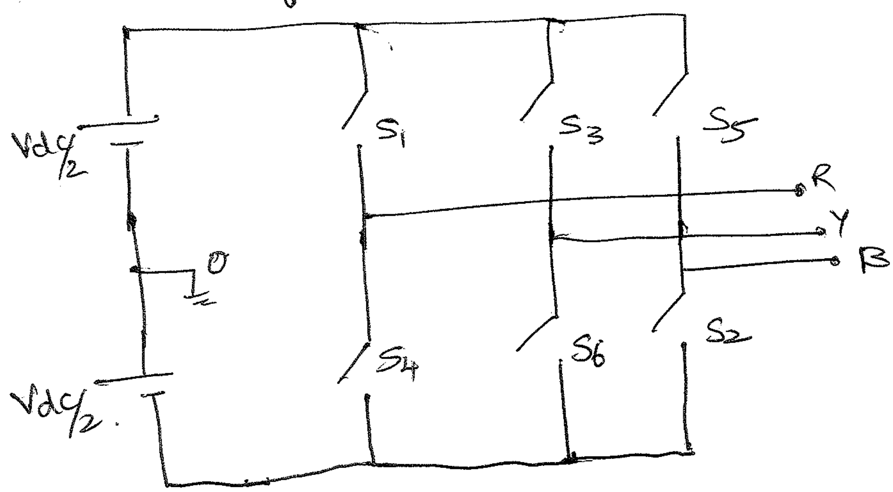
$$V_c = V_m \sin(\omega t + 2\pi/3)$$

When 3 phase AC voltage is applied to AC machine, it produces a rotating air gap flux which can be represented as a single rotating voltage vector. The magnitude and angle of rotating vector can be found by means of clark's transformation

$$\vec{V}_{ref} = V_\alpha + jV_\beta = \frac{2}{3}\left[V_a + aV_b + a^2V_c\right]$$

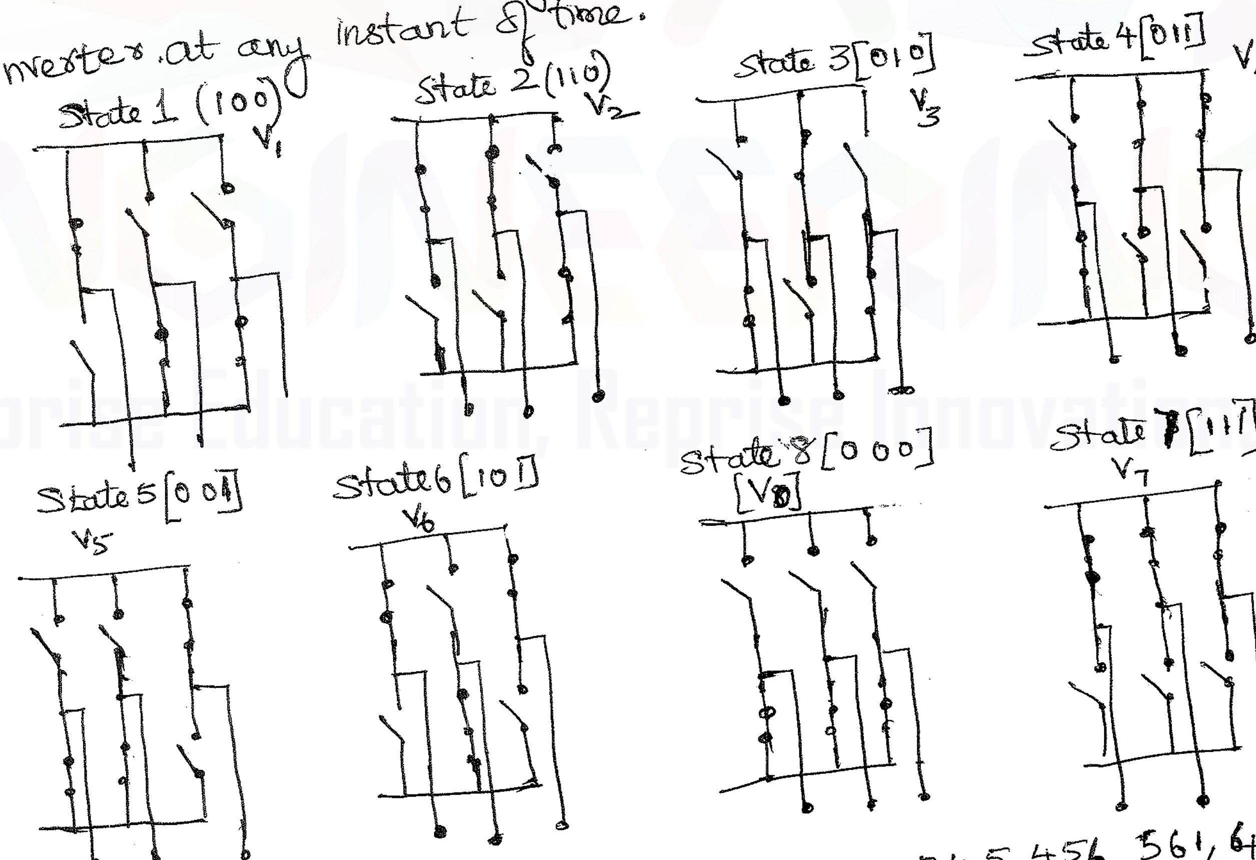
$$a = e^{j2\pi/3} \qquad |V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2} \qquad \phi = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right)$$

Implementation of SVPWM



Consider a three phase voltage source inverter, The ph to centre tap voltage V_{RO}, V_{YO}, V_{BO} have two possible values $V_{DC}/2$, $-V_{DC}/2$ depending on whether the top switch or the bottom switch which is being gated.

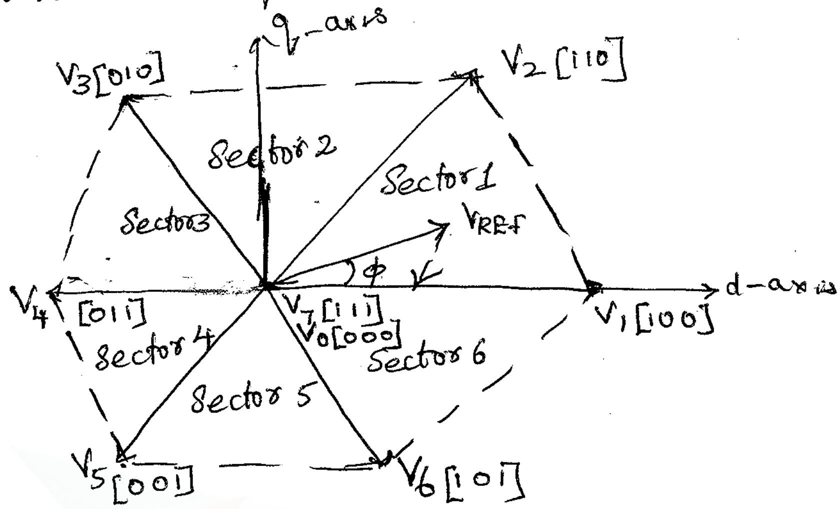
There are eight possible switching states for inverter at any instant of time.



The switching states are 162, 123, 234, 345, 456, 561, 64

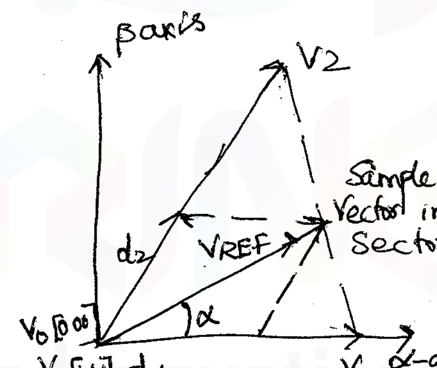
135. ... conducts the vector is taken 1

The phasor of stator voltage stays in each of the positions 1 to 6 for a time interval corresponding to 60° of the fundamental period.



Calculation of Time Variables $[T_1, T_2$ and $T_0]$.

The sampling period is divided into three sub intervals T_1, T_2 and T_0 as shown. The inverter is turned on to produce the vector $\vec{V_1}$ for T_1 seconds, $\vec{V_2}$ for T_2 seconds and Zero vectors ($\vec{V_7}$ (or) $\vec{V_8}$) for T_0 seconds



$$V_{DC} T_1 + V_{DC} \cos 60\, T_2 = |\vec{V_{REF}}| \cos\alpha\, T_s$$

$$T_1 + T_2 \cos 60 = \frac{|V_s^*|}{V_{DC}} T_s \cos\alpha \quad \text{—(1)}$$

$$\alpha = \frac{|V_s^*|}{V_{DC}} \qquad |V_s^*| = |\vec{V_{REF}}|$$

$$V_{DC} \sin 60\, T_2 = |V_s^*| \sin\alpha\, T_s.$$

$$T_2 \sin 60 = \frac{|V_s^*|}{V_{DC}} \sin\alpha\, T_s \quad \text{—(2)}$$

from eq (1) & (2)

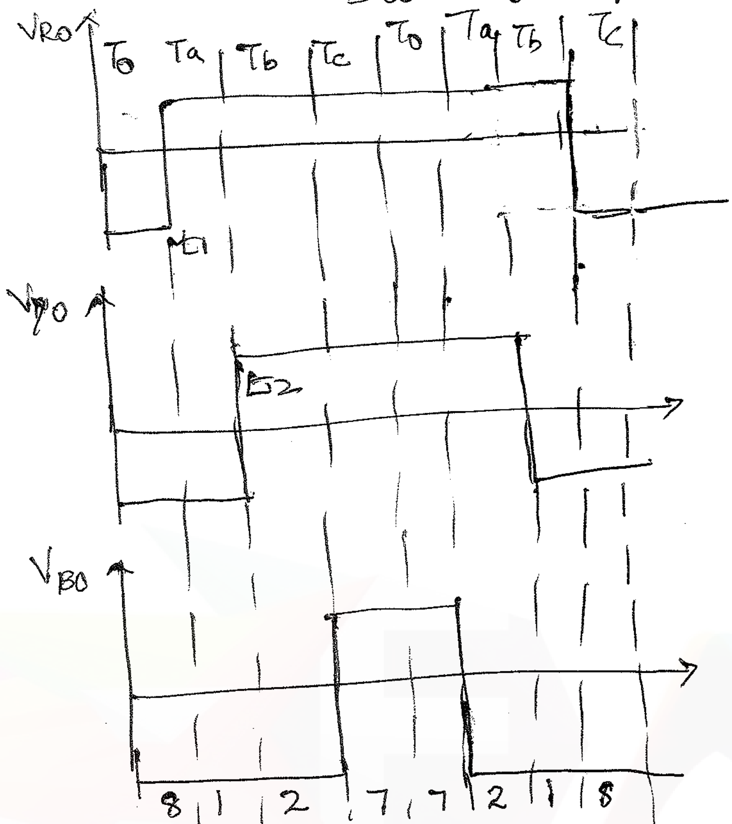
$$T_1 = T_s \alpha \frac{\sin(60-\alpha)}{\sin 60}$$

$$T_2 = T_s \alpha \frac{\sin\alpha}{\sin 60}$$

$$T_0 = T_s = T_1 - T_2.$$

… to another sector the

Determination of switching time for each thyristor in the inverter & Switching sequence



Sector	Time Variables		
	S_1	S_2	S_3
1	$T_0+T_a+T_b$	T_0+T_b	T_0
2	T_0+T_b	$T_0+T_a+T_b$	T_0
3	T_0	$T_0+T_a+T_b$	$T_0+T_a+T_b$
4	T_0	T_0+T_b	$T_0+T_a+T_b$
5	T_0+T_b	T_0	T_0+T_b
6	$T_0+T_a+T_b$	T_0	T_0+T_b

Advantages of SVPWM

1. Excellent output performance
2. Efficiency can be optimized for each load condition
3. By changing the switching behaviour audible noise can be minimized.

Current Source Inverter

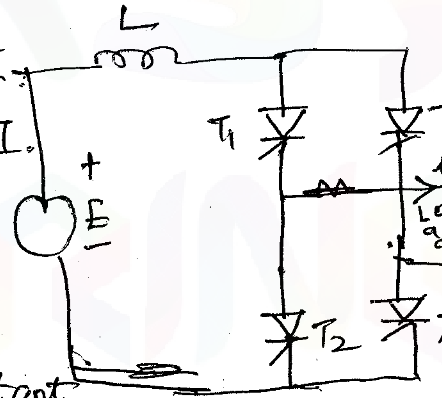
Input voltage is maintained constant and the amplitude of output voltage does not depend upon load. The waveform load current as well as its magnitude depends on the nature of load impedance. In CSI, input current is constant but adjustable. The amplitude of o/p current is independent of load. A CSI does not require any Feedback diodes, whereas they are required in a CSI. Commutation Circuit is simple

CSI find their use in Following applications

(i) Speed control of ac motors
(ii) Induction heating
(iii) Lagging VAR compensation
iv) synchronous motor starting.

Single phase CSI with ideal Switches:-

Thyristor is assumed an ideal switch with zero commutation time. The source consist of inductance and a voltage source. The function of inductance is to maintain constant current at the input terminals of CSI.



when T_1, T_2 are on, i_0 is +Ve, and equal to I.
when T_3, T_4 are On i_0 is −Ve and equal to −I.

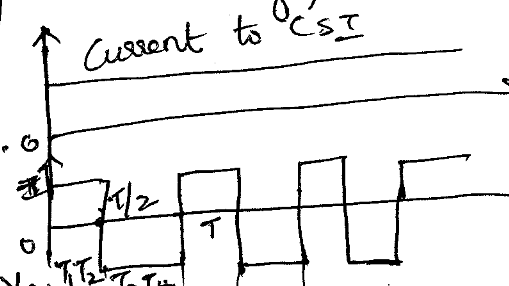
If the load consist of Capacitor C

$$i_0 = C\frac{dv_0}{dt}.$$

i_0 is Constant, slope $\frac{dv_0}{dt}$ must be constant over every half cycle. The slope is positive from 0 to T/2 and negative from T/2 to T.

i/p voltage is positive when T_1, T_2 conduct and it is negative when $T_3 T_4$ conduct.

The dc current input to CSI is unidirectional. If average value of Vin is positive, power flows from to load. In Case average Value of Vin is negative power flows from Load to Source (ie) regeneration of power takes place.

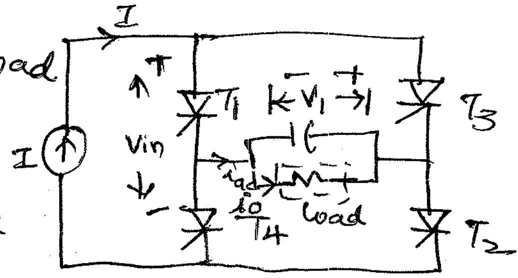


CSI may be load or force Commutated.

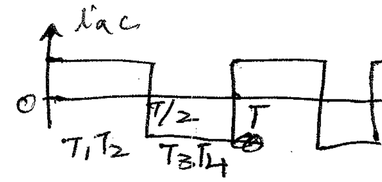
load Commutation takes place when P.f is

Single phase Capacitor Commutated CSI with R load

Capacitor C is in parallel with load for storing the charge for force commutating the SCRs. The thyristors T_1 to T_4 are four power switches.



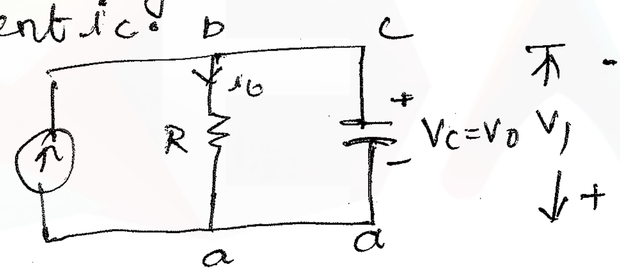
Before $t=0$ let the capacitor voltage be $V_c = -V_1$. (i.e) left hand plate negative and right hand plate positive.



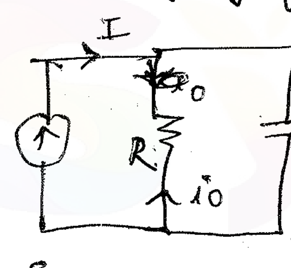
$T_1 T_2$ are gated at $t=0$, capacitor voltage reverse biases conducting thyristors T_3, T_4. So they are commutated immediately.

I now flows through T_1, parallel combination of R and C through T_2.

From 0 to $T/2$, $i_{T_1} = i_{T_2} = I$, $i_{ac} = I$, Capacitor voltage changes from $-V$ to V_1 through the charging by current i_c.



Eq. ckt $0 < t < T/2$



Eq. ckt $T/2 < t <$

Load voltage $V_0 = V_c$.

When T_3, T_4 are gated at $t = T/2$, $V_c = V$, reverse biases and therefore turned off immediately.

Source current flows through T_3, $\parallel^{el}$ combination of R, C and T_4. From $T/2$ to T, $i_{T_3} = i_{T_4} = I$, but $i_{ac} = -I$.

At $t=0$, $V_c = -V_1 = V_0$, load current $i_0 = -\frac{V_1}{R_1} = -I_1$.

from $t=0$ to $T/2$, Capacitor charges from $-V_1$ to V_1.

So $t = T/2$, $i_0 = \frac{V_c}{R} = \frac{V_0}{R} = \frac{V_1}{R} = I_1$.

$$i_0 + i_c = I$$

$$i_c = I - i_0$$

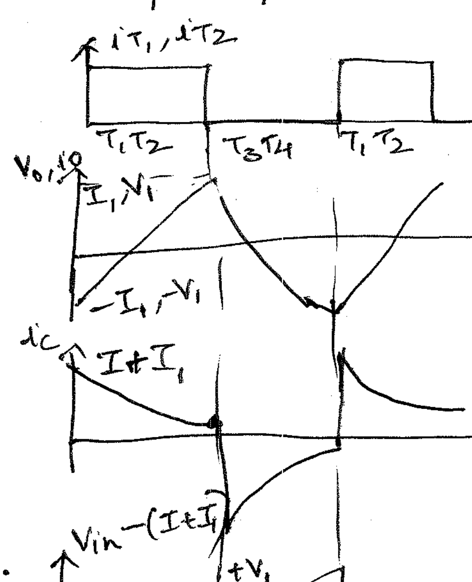
At $t=0$, $i_0 = -I_1$, so $i_c = I + I_1$

before $T/2$ $i_0 = I_1$ $i_c = I - I_1$.

after $t = T/2$, $T_1 T_2$ are off $T_3 T_4$ are conducting

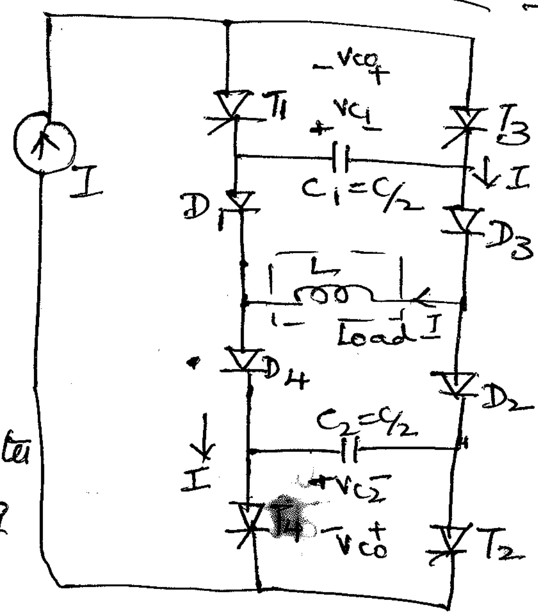
$$i_0 + i_c + I = 0$$

$$i_c = -I - i_0$$



$= -(I+I_1)$.

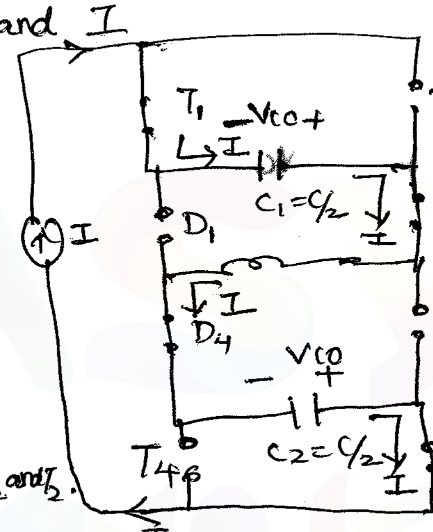
Single phase Auto-Sequential Commutated Inverter (1-ϕ ...)



- Thyristor pair T_1, T_2 and $T_3 T_4$ are alternatively switched to obtain a nearly square wave load current.
- Two Commutating Capacitors, one C_1 in upper half and other C_2 in lower half.
- Diodes D_1 to D_4 are connected in series with each SCR to prevent the Commutation Capacitors from discharging into the load. The inverter o/p frequency is controlled by adjusting the period T through the triggering Circuits of thyristors.

Mode - I:-

Before $t=0$, T_3, T_4 are conducting and a steady current flows through the path $T_3 D_3$, L D_4 T_4 and source I. The Capacitors are charged with polarity $V_{c_1} = V_{c_2} = -V_{co}$.



$t=0$, T_1 and T_2 are on, T_3 T_4 are turned off by reverse capacitor voltage.

$T_1 T_2$ conducts current I. The path for current I is through $T_1, C_1, D_3, L, D_4, C_2$ and T_2. Diodes D_1, D_2 remains reverse biased by V_{co} initially.

$$V_{D1} + V_{co} - \frac{1}{C/2}\int I\, dt = 0$$

$$V_{D1} = -V_{co} + \frac{2}{C}\int I\, dt$$

As the capacitor charges, voltages V_{D1} across D_1 rises lin... Diode D_1 starts conducting. at t_1, V_{D1} becomes zero and diode D_1 ...

$$0 = -V_{co} + \frac{2}{C} I t_1$$

$$t_1 = \frac{C}{2I} V_{co}$$

Capacitor Voltage $V_{C_1} = V_{C_2} = V_C$. appears as reverse voltage acr... thyristors T_3, T_4 when $T_1 T_2$ are gated.

$$V_{C_1} = V_{C_2} = V_C = -V_{co} + \frac{2}{C}\int I\, dt$$

$$= -V_{co} + \frac{2}{C} I t_1$$

$$V_{C1} = V_{C2} = V_C(t_1) = -V_{co} + \frac{2I}{C}\left(\frac{C}{2I} V_{co}\right) = 0$$

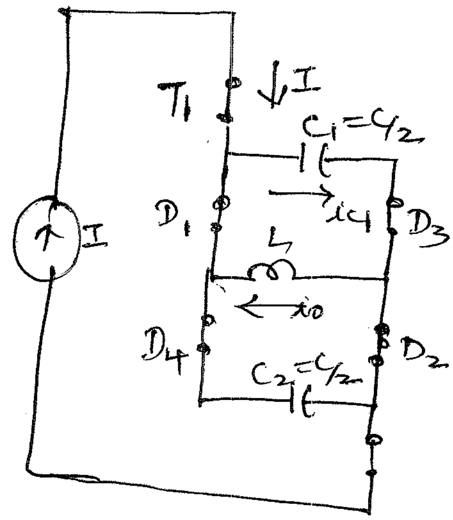
Voltage across C_1, C_2 varies linearly from $-V_{co}$ to zero in time t_1.

Mode II

Diodes D_3, D_4 are already Conducting, but at $t=t_1$ d
D_1, D_2 get forward biased and start conducting. Thus at en
time t_1, all four diodes D_1, D_2, D_3 and D_4 Conduct. So
Commutating Capacitors now get connected in ||el with

$$I + i_0 = i_c \left(= i_{c1} + i_{c2}\right)$$

$$i_{c1} = i_{c2}, \quad i_{c1} = i_{c2} = \frac{1}{2} i_c$$



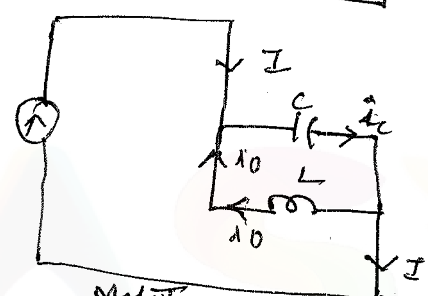
$$L\frac{di_0}{dt} + \frac{1}{C}\int i_c \, dt = 0$$

$$L\frac{di_0}{dt} + \frac{1}{C}\int (I + i_0)\, dt = 0$$

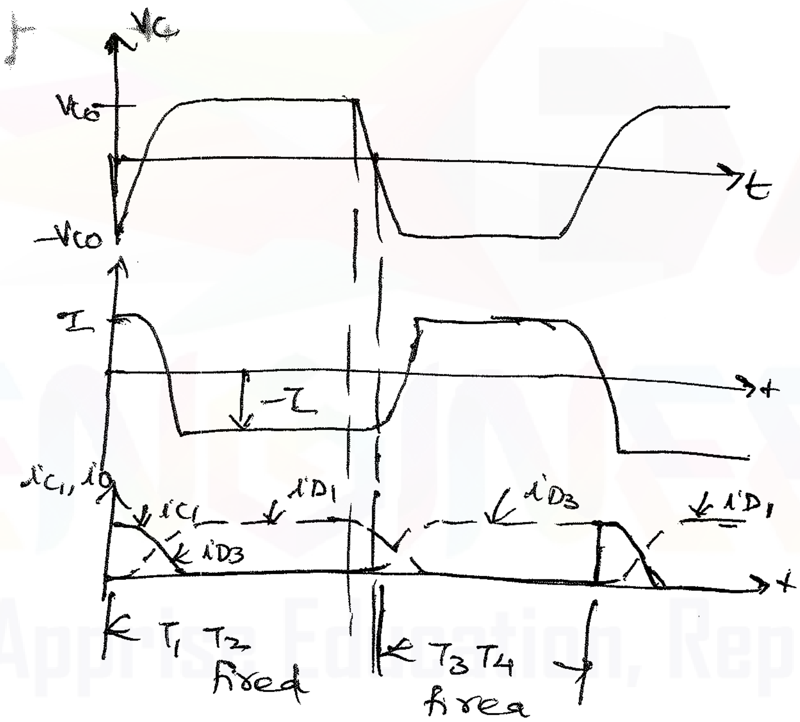
$$L\frac{d^2 i_0}{dt^2} + \frac{i_0}{C} = -\frac{I}{C}.$$

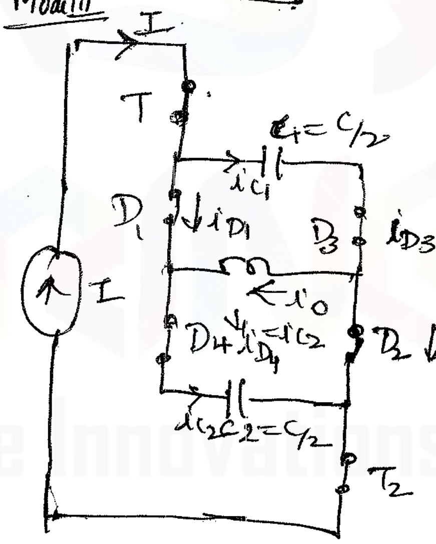
at $t=0$

$$I_0 = I \text{ and } \frac{di_0}{dt} = 0$$



Mode III

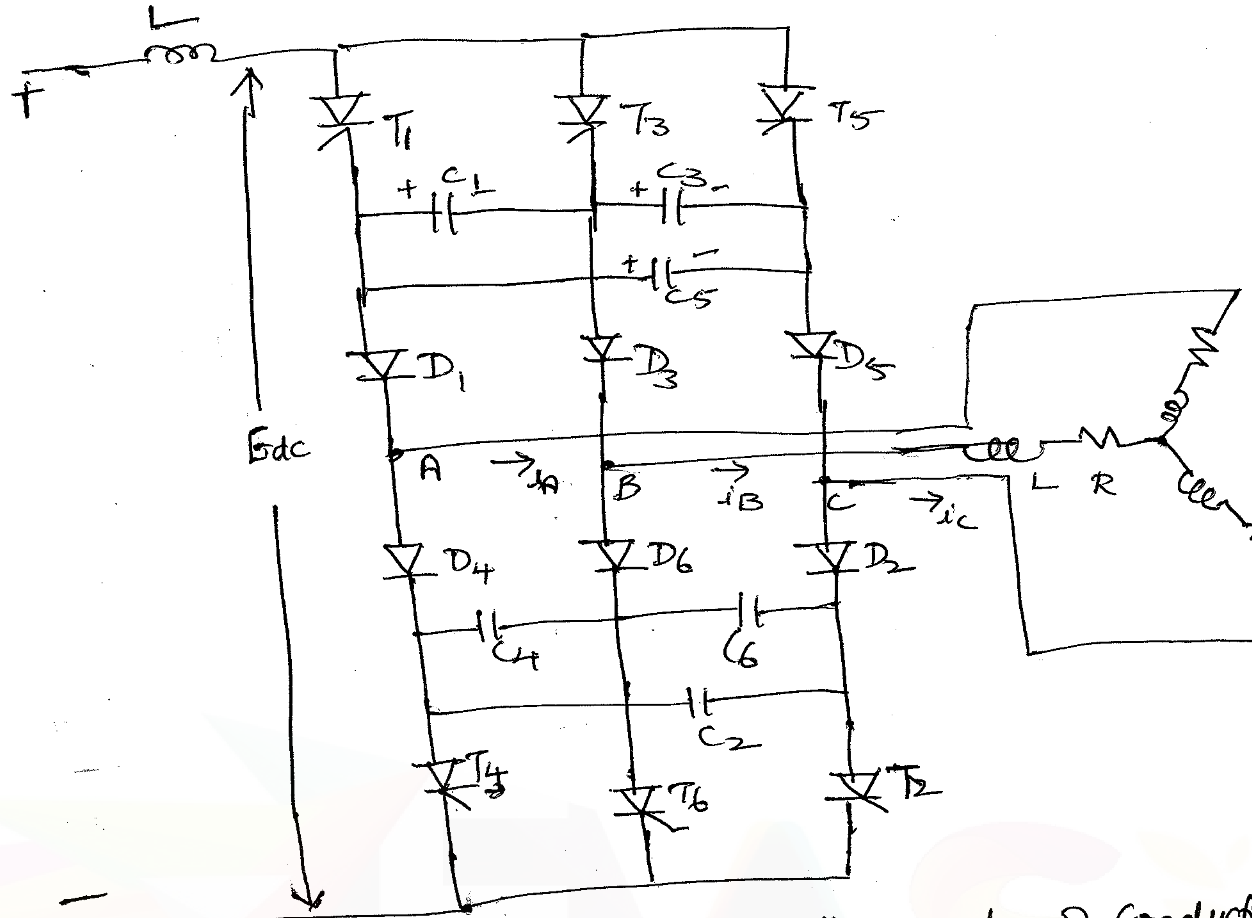




Mode - IV

At the end of total Commutation interval (t_1+t_2) stea
i/p current I flows through T_1, D_1, Load L, D_2 and T_2.
This constant current continues to flow till the next Commut
process is gated by T_3 and T_4.

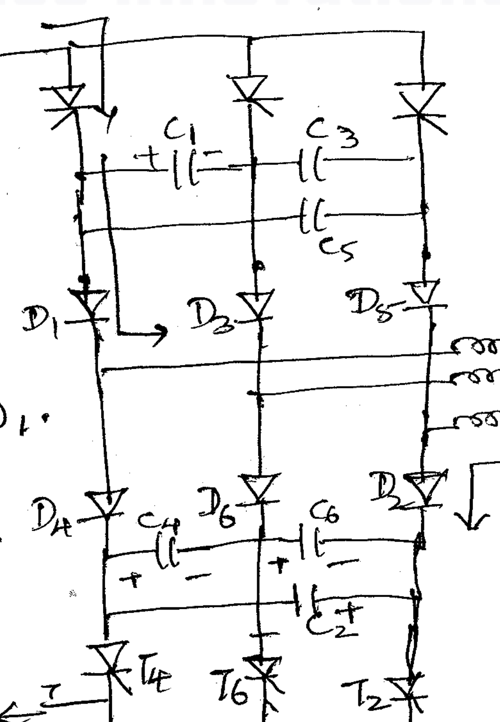
Three phase Auto sequential Commutated Inverter



Six thyristors T_1 to T_6 are gated in the order of conduct
each thyristor conducts for 120° of o/p period. Six blocking diod
D_1 to D_6 isolate the capacitors from the load.

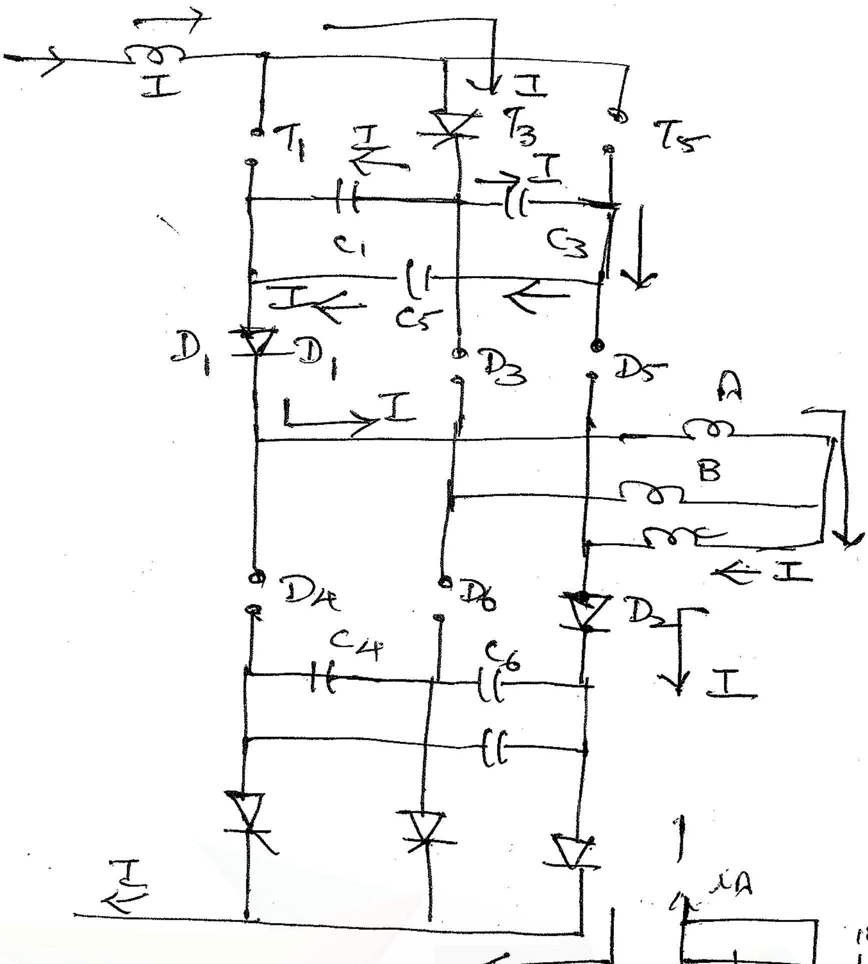
Mode-I:

T_1 T_2 have been conducting for some time, so that phase A and C carry current but phase B does not. Capacitors C_1, C_3 and C_5 are charged with voltage E_L, Zero a $-E_L$ respectively. When the inverter is first switched on, Cap must be precharged with a voltage distribution of this nature.

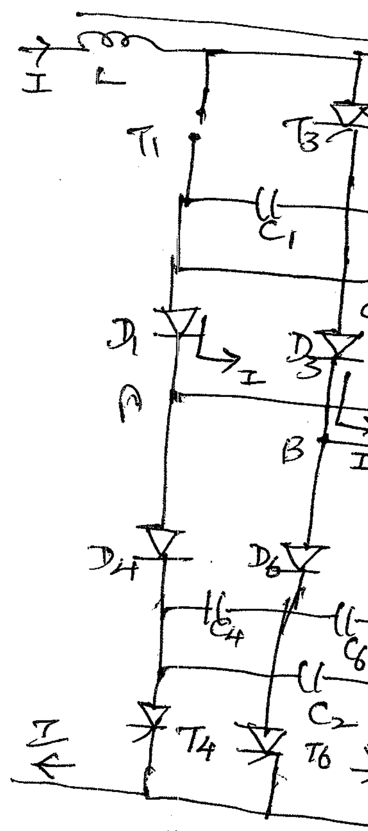


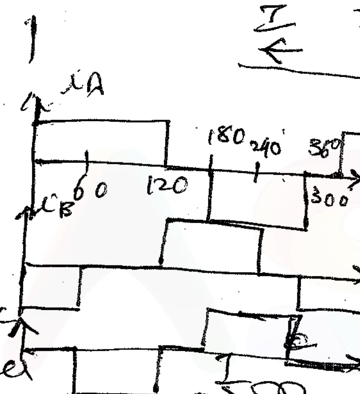
Mode-2

T_3 is triggered, T_1 is R.B by voltage on capacitor C_1 and then off. The current I which was flowing through T_1 is now flowing through T_3. Capacitor bank formed by C in parallel with C_3 and C_5 and diode D_1. During charging period the current Source I linearly charges the capacitor bank. The outgoing thyristor T_1 is R. B until another phase. Current have same



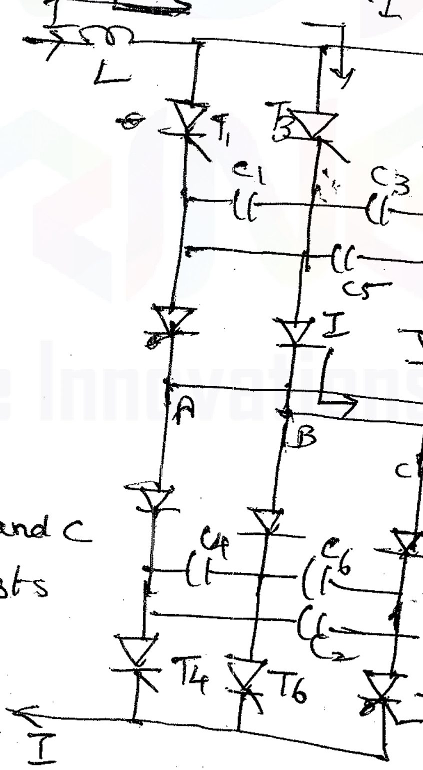
Mode II





Mode 3 :

when diode D_3 conducts the upper capacitor is ||el with the motor through diodes D_1 and D_3. The LC circuit resonates in one quarter of the resonant period, the oscillatory current reduces the phase A current from I to zero, and increases the phase B current from zero to I.



Mode 4

Mode 4 ::

Source current I now flows through B and C through thyristors T_3 and T_2. This condition lasts untill T_4 is gated to initiate the next commutation. D_3 is the only conducting diode in the upper group, upper capacitor group retains its charge untill the next upper group commutation.

Advantages of CSI

(i) Capable of regeneration
(ii) DC link filter inductor and RPS acts as current limiter

Disad

(1) filter inductor is cos... and more losses are f...
(2) High voltage spikes...

UNIT-V

Ac-Ac Converters

Ac Voltage Controllers:

It is a thyristor based devices which conver[ts] fixed alternating voltage directly to variable alternating voltag[e] without a change in the frequency.

Applications:

Domestic and Industrial heating, Transformer tap chang[ing], lighting control, speed control of single phase and three ph[ase] ac drives, and starting of induction motors.

Disadvantage of Ac Voltage controller:-

Introduction of objectionable harmonics in the su[pply] current and load voltage waveforms, particularly at reduced output voltage levels.

Types of Power Transfer:

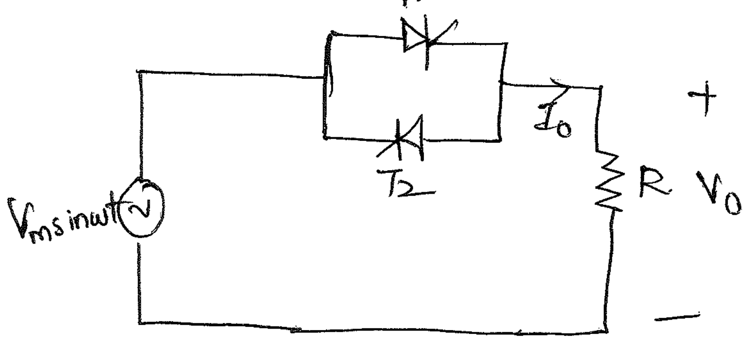
1. ON-off control
2. Phase Control

ON-OFF Control:

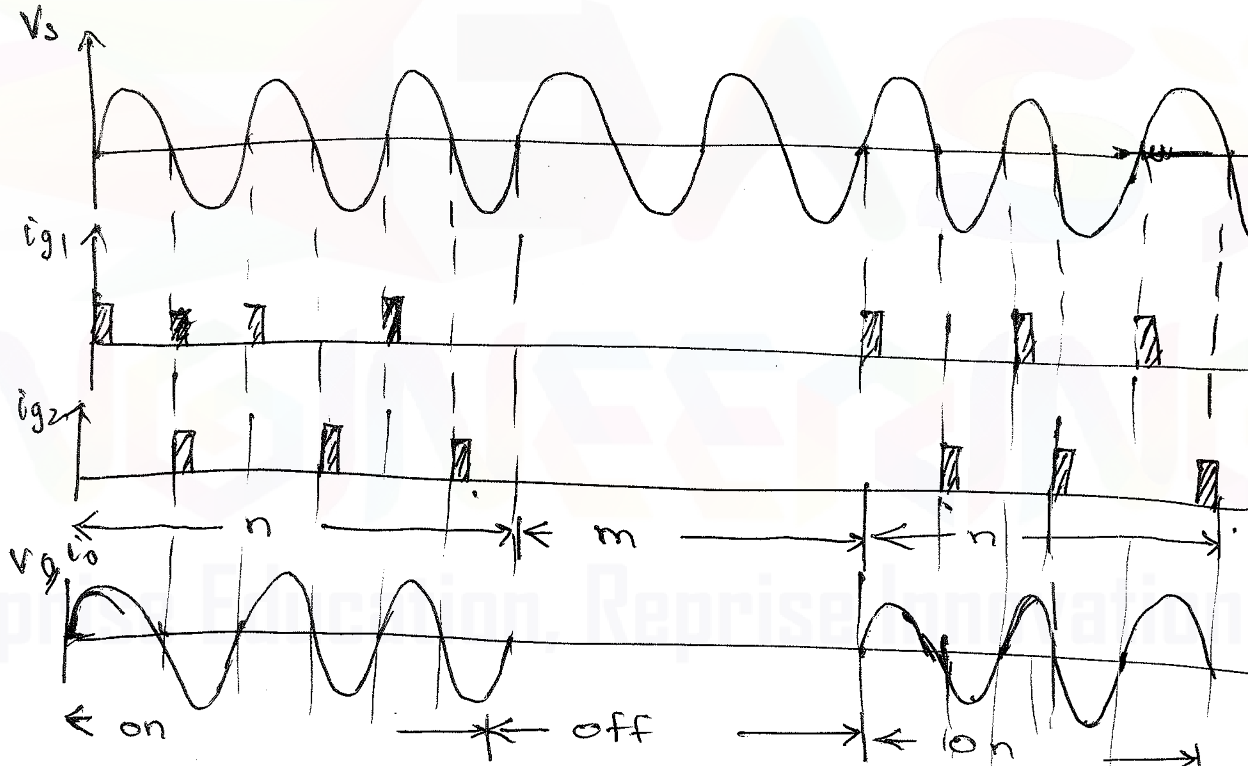
Thyristors are employed as switches to co[nnect] the load circuit to the source for a few cycles of sourc[e] voltage and disconnect it for another few cycles. This [is] known as on-off control or Integral cycle control.

* In industries there are several applica[tions] in which mechanical time constant or thermal time consta[nt] is in order of several seconds which may be very large. [...] there will be no variati[on]

* For such applications if control is achieved by con[necting] the load to source for few cycle and then disconne[cting it] for another few cycles. This form of power control is [known as] Integral cycle control.



Two thyristors are connected in antiparallel and turned on by gate pulse i_{g1}, i_{g2} at zero voltage crossing of supply voltage. The source energises load for (n = 3) cycles. When gate pulses are removed load remains off for (m = 2) cycles. By this method of turn and turn off the load power is controlled.



In literature integral cycle control is known as on-off burst firing, zero voltage switching, cycle selection or cycle syncopation.

RMS value of output voltage V_{or}

$$V_{or} = \frac{1}{\text{Periodicity}}\left[\int_0^{2\pi} V_m^2 \sin^2 wt\,(dwt) \text{ for first on cycle} + \int_{2\pi}^{2\pi} V_m^2 s\ldots\right.$$

$$V_{or} = \left[\frac{n}{2\pi(n+m)} \int_0^{2\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= \left[\frac{n V_m^2}{4\pi(n+m)} \int_0^{2\pi} (1 - \cos 2\omega t) \, d\omega t\right]^{1/2}$$

$$V_{or} = \frac{V_m}{\sqrt{2}} \sqrt{\frac{n}{n+m}} = V_s \sqrt{\frac{n}{n+m}} = V_s \sqrt{k}$$

$k = \frac{n}{n+m}$ is the duty cycle of ac voltage controller.

RMS load current $I_{or} = \frac{V_{or}}{R}$

Power delivered to load $= \frac{V_{or}^2}{R} = \frac{V_s^2}{R}\left(\frac{n}{n+m}\right) = K \frac{V_s^2}{R}$

RMS value of input current I_s = rms value of load current

Input VA $= V_s I_s = V_s I_{or} = V_s \frac{V_{or}}{R}$

Input VA × P.f = Power delivered to load

$$\text{Input P.f} = \frac{V_{or}^2}{R} \cdot \frac{R}{V_s \cdot V_{or}} = \frac{V_{or}}{V_s} = \sqrt{\frac{n}{n+m}} = \sqrt{K}$$

Average Thyristor current

$$I_{TA} = \frac{1}{2\pi} \int_0^{\pi} I_m \sin \omega t \, d\omega t \text{ (first cycle)} + \frac{1}{2\pi} \int_0^{\pi} I_m \sin \omega t \text{ (second cycle)}$$

$$+ \cdots + \frac{1}{2\pi} \int_0^{\pi} I_m \sin \omega t \text{ for } n \text{ cycle.}$$

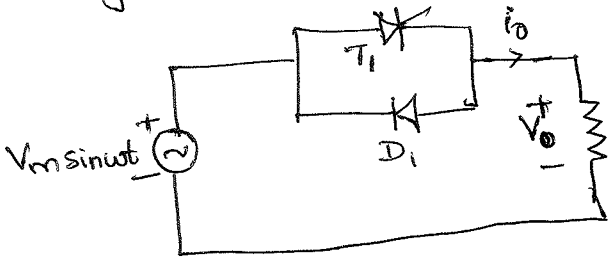
$$= \frac{n}{2\pi(n+m)} \int_0^{\pi} I_m \sin \omega t \, d\omega t = \frac{I_m}{\pi} \frac{n}{n+m} = k \frac{I_m}{\pi}$$

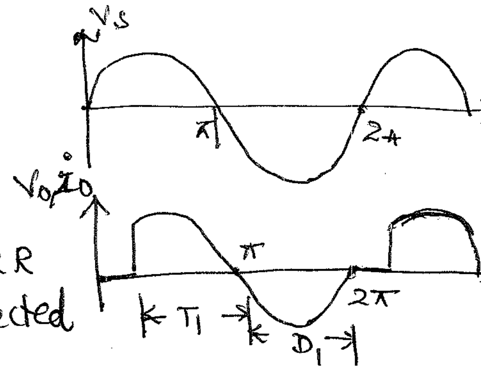
RMS value of thyristor current

$$I_{RR} = \left[\frac{n}{2\pi(n+m)} \int_0^{\pi} I_m^2 \sin^2 \omega t \, d\omega t\right]^{1/2}$$

$$= \frac{I_m}{2} \sqrt{\frac{n}{n+m}} = \frac{I_m \sqrt{k}}{2}$$

Single phase Half wave AC voltage controller





The circuit consists of one SCR and one diode D_1, which are connected in antiparallel.

During positive half cycle thyristor T_1 is forward

At $\omega t = \alpha$, T_1 is turned on positive gate pulse. The load current flows

T_1 is conducting upto $\omega t = \pi$,

$P - T_1 - R - N$.

At $\omega t = \pi$, supply voltage falls to zero. Hence T_1 is

off by natural commutation.

$\omega t = \pi$, D_1 is forward biased and it conducts till

The load current flows through $N - R - D_1 - P$.

$$V_{orms} = \left[\frac{1}{2\pi}\left[\int_{\alpha}^{\pi} V_m^2 \sin^2\omega t \, d\omega t + \int_{\pi}^{2\pi} V_m^2 \sin^2\omega t \, d\omega t\right]\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\left[\int_{\alpha}^{\pi} \sin^2\omega t \, d\omega t + \int_{\pi}^{2\pi} \sin^2\omega t \, d\omega t\right]\right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi}\left[\int_{\alpha}^{\pi}(1 - \cos 2\omega t)\right] d\omega t + \int_{\pi}^{2\pi}(1 - \cos 2\omega t) \, d\omega t\right]^{1/2}$$

$$V_{orms} = \frac{V_m}{2}\left[\frac{1}{\pi}\left(2\pi - \alpha\right) + \frac{\sin 2\alpha}{2}\right]^{1/2}$$

$$I_{orms} = \frac{V_{orms}}{R}$$

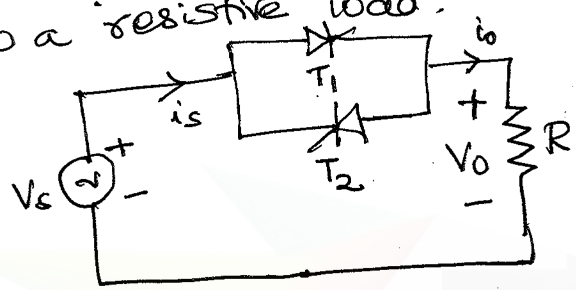
$$V_0 = \frac{1}{2\pi}\left[\int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t + \int_{\pi}^{2\pi} V_m \sin\omega t \, d\omega t\right]$$

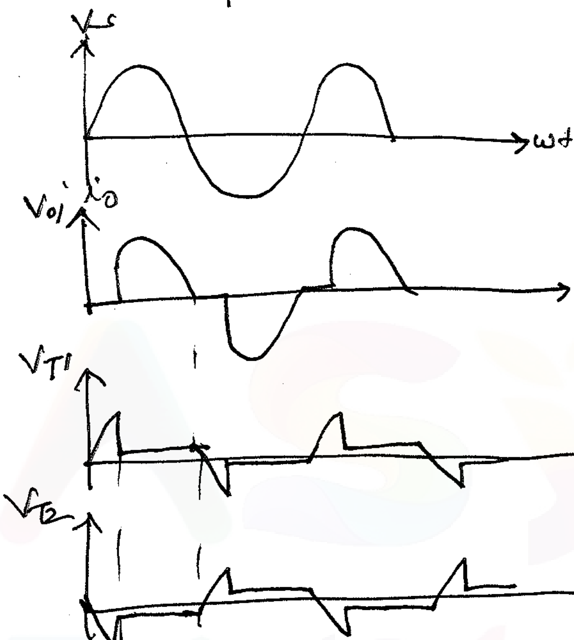
$$P.f = \frac{I_{orms}^2 R}{V_s I_{orms}}$$

$$\boxed{P.f = \frac{I_{orms} R}{V_s}}$$

Single phase full wave Ac voltage controller

Two thyristors are connected in antiparallel are conn[ected] to a resistive load.





T_1 and T_2 are forward biased during positive and negative half cycles respectively.

During positive half cycle,

T_1 is triggered at firing angle α.

The load voltage flows through V_s^+, T_1, R, V_s^-.

At $\omega t = \pi$, V_o, i_o falls to Zero T_1 is turned off.

During negative half cycle T_2 is triggered at $(\pi+\alpha)$,

T_2 conducts from $\pi+\alpha$ to 2π.

T_2 is subjected to a reverse bias, it is therefore comm[utated].

$$V_{orms} = \left[\frac{1}{\pi}\int_\alpha^\pi V_m^2 \sin^2\omega t \, d\omega t\right]^{1/2} = \left[\frac{V_m^2}{2\pi}\int_\alpha^{\pi}(1-\cos 2\omega t)\, d\omega t\right]^{1/2}$$

$$= V_m\left[\frac{1}{2\pi}(\pi-\alpha)+\frac{\sin 2\alpha}{2}\right]^{1/2}$$

$$I_{orms} = \frac{V_{orms}}{R}$$

$$I_{... } = \frac{1}{...}\left[\int^{\pi} ... \right]^{1/2} \left(\frac{V^2}{...}\right) ... \cos 2\omega t) d...$$

$$= \frac{V_m}{2R}\left[\frac{1}{\pi}(\pi-\alpha)+\frac{\sin 2\alpha}{2}\right]^{1/2}$$

Average thyristor Current $I_{TA} = \left[\frac{1}{2\pi R}\int_{\alpha}^{\pi} V_m \sin\omega t\right.$

$$= \frac{V_m}{2\pi R}(\cos\alpha + 1)$$

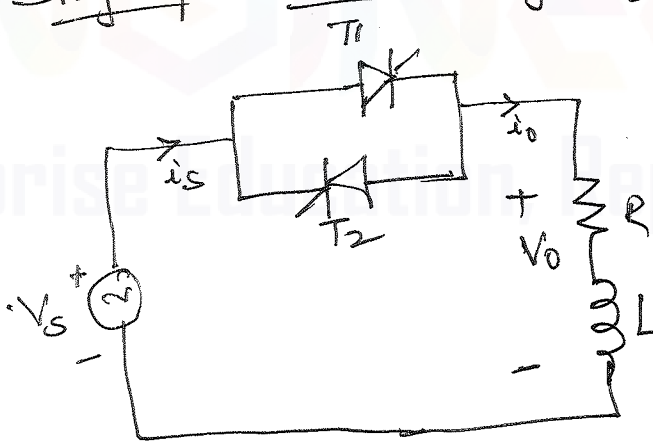
Input P.f $= \frac{P_o}{VA} = \frac{V_{orms}^2}{R\ V_s\ I_{orms}}$

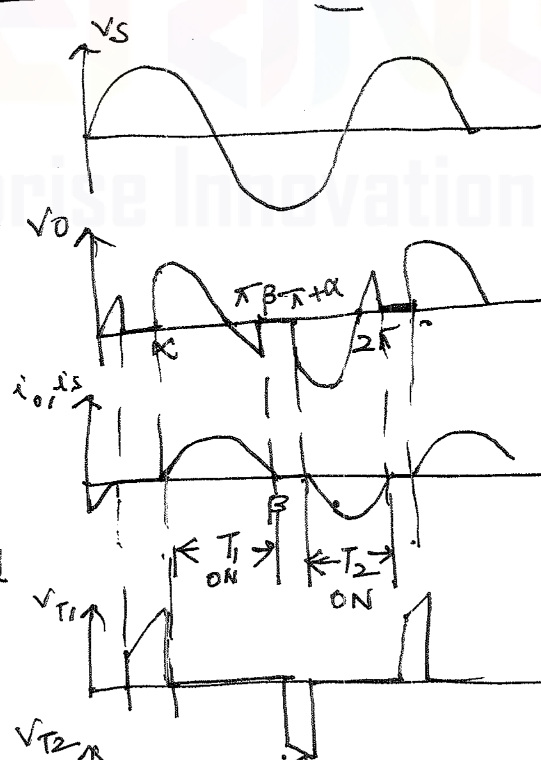
$$= \frac{V_{orms}^2}{R\,V_s\,\frac{V_{orms}}{R}}$$

$$P.f = \frac{V_{orms}}{V_s} = \frac{V_{orms}}{V_s}.$$

$$P.f = \frac{1}{\pi}\left(\pi-\alpha+\frac{\sin 2\alpha}{2}\right]^{1/2}$$

Single phase Ac Voltage Controller with RL load





Single phase Full wave AC Voltage controller with RL load is divided into three Cases

(i) $\alpha > \phi$ (ii) $\alpha = \phi$ (iii) $\alpha < \phi$

Displacement angle is defined as the angle between t
Fundamental Component of ac line Current and the associated line to neutral Voltage.

(i) $\alpha > \phi$.

During positive half cycle, T_1 is F.B,
$\omega t = \alpha$, T_1 is triggered. $i_0 = i_{T_1}$ starts building up through the load.

At $\omega t = \pi$, $V_0 = V_s = 0$ but load current is not zero because of the presence of inductance in the load.. T_1 Continues to conduct untill current falls to zero at
Angle β is called extinction angle.

from β to $\pi + \alpha$, load is isolated from source, T_1 and T are turned off.

During negative half cycle T_2 is F.B
At $\omega t = (\pi + \alpha) > \beta$, T_2 is triggered, $i_0 = i_{T_2}$ starts building up in reverse direction through the load.
At $\omega t = 2\pi$, $V_0 = V_s = 0$, but $i_{T_2} \neq 0$. At $\omega t = \pi + \alpha$-
$i_{T_2} = 0$, T_2 is turned off because it is reverse biase
Here γ is the conduction angle.

from $(\pi + \alpha + \gamma)$ to $(2\pi + \alpha)$, load is isolated from the Source.

$$V_{orms} = \left[\frac{2}{2\pi} \int_{\alpha}^{\beta} V_m^2 \sin^2 \omega t \, d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} (1 - \cos 2\omega t \, d\omega t)\right]^{1/2}$$

For $\alpha \leq \omega t \leq \beta$ KVL equation is given as

$$R i_o + L\frac{di_o}{dt} = V_m \sin\omega t$$

$$i_o = \frac{V_m}{Z}\sin(\omega t - \phi) + A e^{-(R/L)t} \quad \text{—(1)}$$

$$Z = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

$i_o = 0$, $\omega t = \alpha$, $t = \alpha/\omega$

$$0 = \frac{V_m}{Z}\sin(\alpha - \phi) + A e^{-R\alpha/\omega L}$$

$$A = -\frac{V_m}{Z}\sin(\alpha - \phi)\, e^{R\alpha/\omega L}$$

Sub A in eq (1)

$$i_o = \frac{V_m}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)\, e^{\frac{R}{L}\left(\frac{\alpha}{\omega} - t\right)}\right]$$

load current falls to zero at an angle $\omega t = \beta$.

$$\sin(\beta - \phi) = \sin(\alpha - \phi)\, e^{\frac{R}{L}\left(\frac{\alpha - \beta}{\omega}\right)}$$

$$\gamma = \beta - \alpha$$

(ii) $\alpha = \phi$.

From 0 to α – T_2 ON

α to $\pi + \alpha$ T_1 ON

$\pi + \alpha$ to $2\pi + \alpha$ T_2 ON

load current never becomes zero and load is always connected to source. when $\gamma = \phi$, load is directly connected to source.

For an RL load with load phase angle ϕ, the load current will be a sine wave and lag behind the ... by an angle ϕ. From 0 to ϕ – T_2 ON

(iii) $\alpha < \phi$

T_1 will not get turned on because it is reverse biased by voltage drop in SCR T_2 which is conducting current i_{T_2}. T_1 will get turned on only at ϕ when (
T_1 will conduct from ϕ to $(\pi+\phi)$.

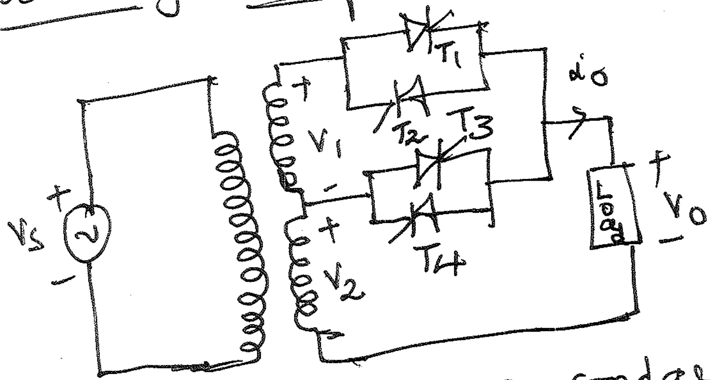
T_2 will be triggered at an angle $(\pi+\alpha) < (\pi$
T_1 is conducting a voltage drop in T_1 will apply across
as a result T_2 will not be turned on at $(\pi+\alpha)$.
$i_{T_1} = 0$, at $(\pi+\phi)$.
T_2 conduct from $(\pi+\phi)$ to $(2\pi+\phi)$

A reduction of angle ϕ below will not contro
the output voltage and current. The ac output powe
can be controlled only for $\alpha > \phi$. Thus the control range
delay or firing angle is $\phi < \alpha < \pi$.

Sequence control of AC Voltage Controllers (Transforme Tap change

* Sequence control is used for the improvemen system power factor and for the reduction of harmonics in the input current and output voltage.
* Sequence control means two or more stages o voltage controllers in parallel for the regulati of output voltage.
* The term sequence control means the stage voltage controllers in parallel are triggered proper sequence one after the other to obta
... with low harmonic content

Two stage Sequence Control of Voltage Controllers



The turns ratio from primary to seconda[ry] taken as unity.

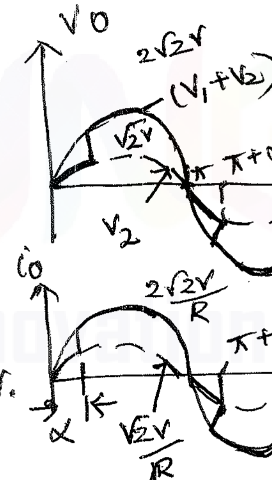
$V_1 = V_2 = V_m \sin\omega t$

* The sum of two secondary voltage is $2V_m$
* The load is of R and RL.
* To obtain an o/p voltage from 0 to RMS value V, $T_3 T_4$ are turned on
* To obtain an output voltage from V to $2V$, T_1 [T_2] are turned on where α is varied from 0 to 180

Advantages:

Reduction of harmonics in the load and line curr[ent]

Resistance load :-



The load Current and voltage waveforms are identical for resisitive load. When both pairs ($T_1 T_2$, $T_3 T_4$) are in operation, firing angle for T_3, T_4 is always zero whereas firing angle α for pair $T_1 T_2$ is varied from 180 to zero for o/p voltage from V to $2V$.

At $\omega t = 0$, T_3 is triggered the output voltage follows V_2

At $\omega t = \alpha$ T_1 is triggered V_1 reverse biases T_3 and it is [turned off]

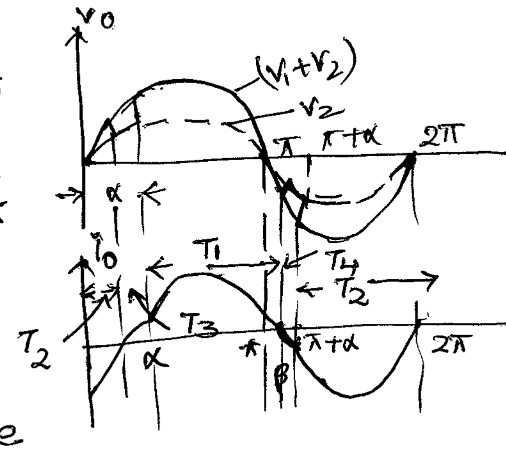
the o/p voltage jumps from V_2 to (V_1+V_2) and follows $2V_m \sin\omega t$

At $\omega t = \pi$, o/p voltage and current are zero.

$\omega t = \pi$, T_4 is triggered and o/p voltage follows $V_m \sin\omega t$ curr[ent]

$\omega t = \pi + \alpha$, SCR T_2 is triggered and T_4 is reverse biased and hen[ce]

RL Load



During positive half cycle T_3 is conducting and a voltage V_2 is applied to load.

$\omega t = \alpha$, T_1 is triggered, T_3 is turned off by reverse voltage V_1 and output voltage jumps to $V_1 + V_2 = 2V_m \sin\omega t$.

At $\omega t = \pi$, (V_1+V_2) reaches zero but output current i_o is not zero because of the presence of L in the load.

T_1 continues conducting until $\omega t = \beta$ where i_o decays to zero. T_1 is turned off.

At $\omega t = \pi$, T_4 starts conducting lower the voltage V_2.

At $\omega t = \pi + \alpha$, T_2 is triggered and V_1 turns off T_4 and the output voltage jumps to (V_1+V_2) in negative half cycle.

At $\omega t = 2\pi$, (V_1+V_2) reaches zero but i_o is not zero becau[se] of L.

At $\omega t = \pi + \beta$, i_o reaches zero, T_2 is turned off. and the cycle repeats.

Multistage Sequence Control of Voltage Controllers:

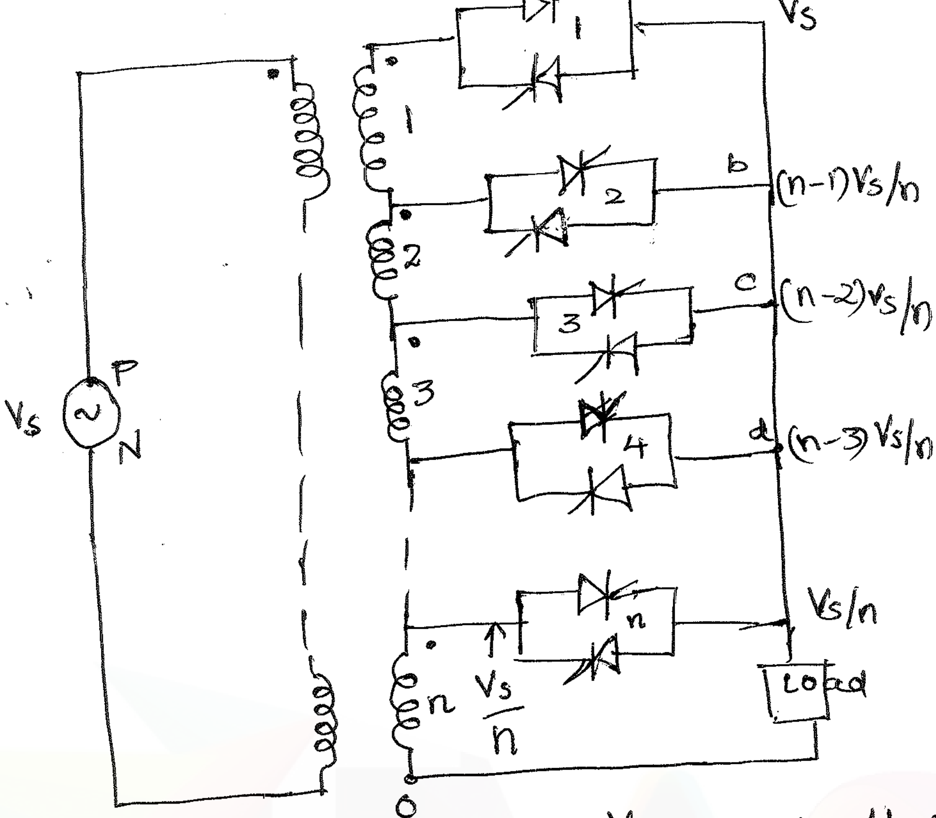
It is employed when it is desired to have harmonic content lower than that in a two stage sequence control. The transformer has n secondary windings. Each secondary winding is rated as V_s/n. Voltage of terminal a with respect to 0 is V_s.

Voltage of terminal b is $(n-1)V_s/n$.

Voltage control from $V_{do} = (n-3)V_s/n$ to $V_{co} = (n-2)V_s/n$.

Thyristor pair 4 is fired at $\alpha = 0°$.

Thyristor pair 3 is controlled from $\alpha = 0$ to $180°$ whereas al[l]



For Controlling the output Voltage V_{bo} to V_{ao} thyristor pair is triggered at $\alpha = 0$, Thyristor pair 1 is ... from 0 by keeping the remaining (n-2) SCR pairs off.

The load voltage can be controlled from Vs/n to Vs.

Presence of harmonics in the output voltage ... upon the magnitude of voltage variation. If voltage variation is a small fraction of total output voltage the harmonic content in the output voltage is small.

Three phase Ac Voltage Controller:-

It is a converter circuit which converts 3phase Ac to 3 phase variable voltage without change in supply frequency.

Two types of 3phase Ac Voltage controllers or regulators

1. Unidirectional Controller 2. Bidirectional Controller.

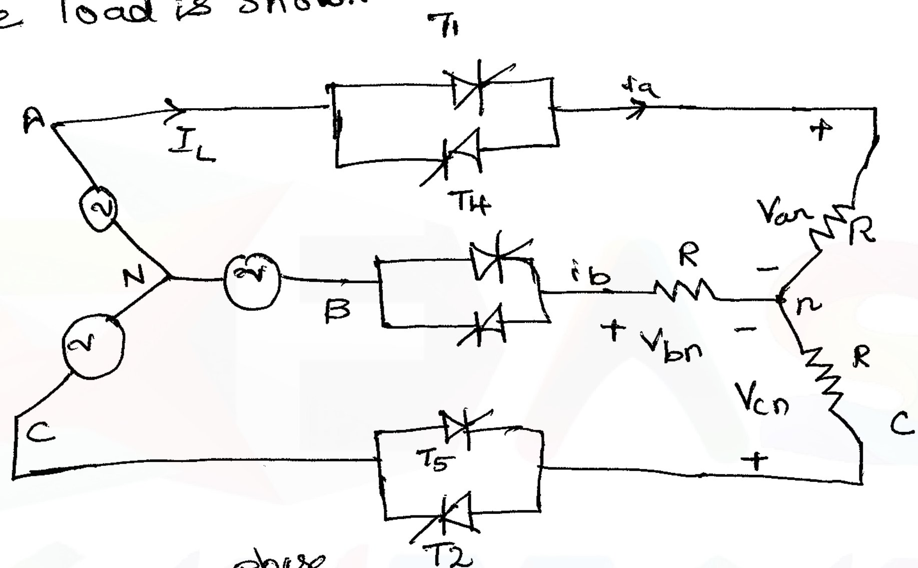
Unidirectional Controller is not preferred because of

Bidirectional controllers are of two types namely

1. Three phase Bidirectional star connected load
2. Three phase bidirectional delta connected load.

Three phase Bidirectional or full wave ac controller f... star connected load

Three phase full wave controller for star connec... resistive load is shown



The instantaneous phase i/p voltage as $V_{AN} = \sqrt{2} V_s \sin\omega t$

$$V_{BN} = \sqrt{2} V_s \sin(\omega t - 2\ldots$$

$$V_{CN} = \sqrt{2} V_s \sin(\omega t - 4\pi/3)$$

The instantaneous line voltages are

$$V_{AB} = \sqrt{6} V_s \sin(\omega t + \pi/6)$$

$$V_{BC} = \sqrt{6} V_s \sin(\omega t - \pi/2)$$

$$V_{CA} = \sqrt{6} V_s \sin(\omega t - 7\pi/6).$$

For $0 \leq \alpha \leq 60°$

Two thyristors conducts before the firing of T_1. Once T_1 is fired three thyristor conducts. A thyristor is turn... off when its current attempts to reverse. The conditions for $60^\circ \le \alpha < 90^\circ$

Two thyristor conducts at any time.

for $90^\circ \le \alpha \le 150^\circ$, Two thyristors conduct at any time there are periods when no thyristors are on.

for $\alpha \ge 150^\circ$, no period for two conducting SCR and o/p Vo becomes Zero at $\alpha = 150^\circ$. The range of delay angle is

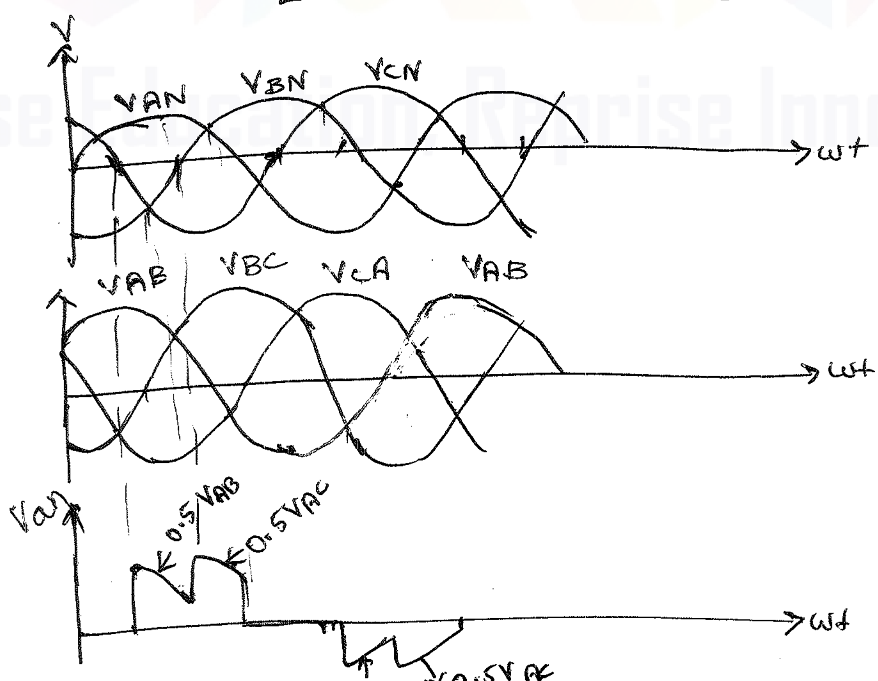
$0 \le \alpha \le 150^\circ$

for $0 \le \alpha \le 60^\circ$

$$V_o = \frac{1}{2\pi}\int_0^{2\pi} V_{an}^2 \, d(\omega t)$$

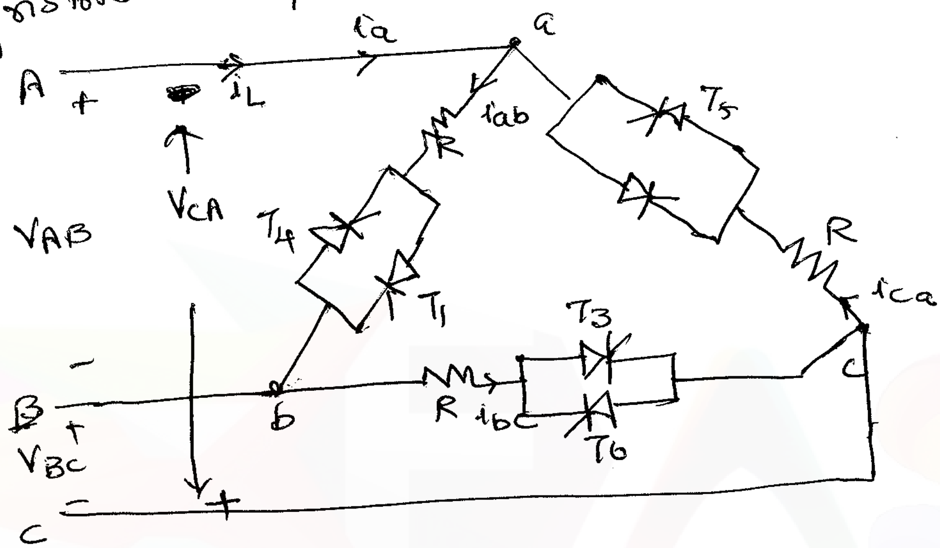
$$= \sqrt{6} V_s \left\{ \frac{2}{2\pi} \int_{\alpha}^{\pi/3} \frac{\sin^2\omega t}{3} d\omega t + \int_{\pi/4}^{\pi/2+\alpha} \frac{\sin^2\omega t}{4} d\omega t + \int_{\pi/3+\alpha}^{2\pi/3} \frac{\sin^2\omega t}{3} d\omega t + \int_{\pi/2}^{\pi/2+\alpha} \frac{\sin^2\omega t}{4} d\omega t + \int_{2\pi/3+\alpha}^{\pi} \frac{\sin^2 \ldots}{3} \ldots \right.$$

$$= \sqrt{6} V_s \left[\frac{1}{\pi}\left(\frac{\pi}{6} - \frac{\alpha}{4} + \frac{\sin 2\alpha}{8}\right)\right]^{1/2}$$



Three phase Bidirectional Delta Connected Controller:

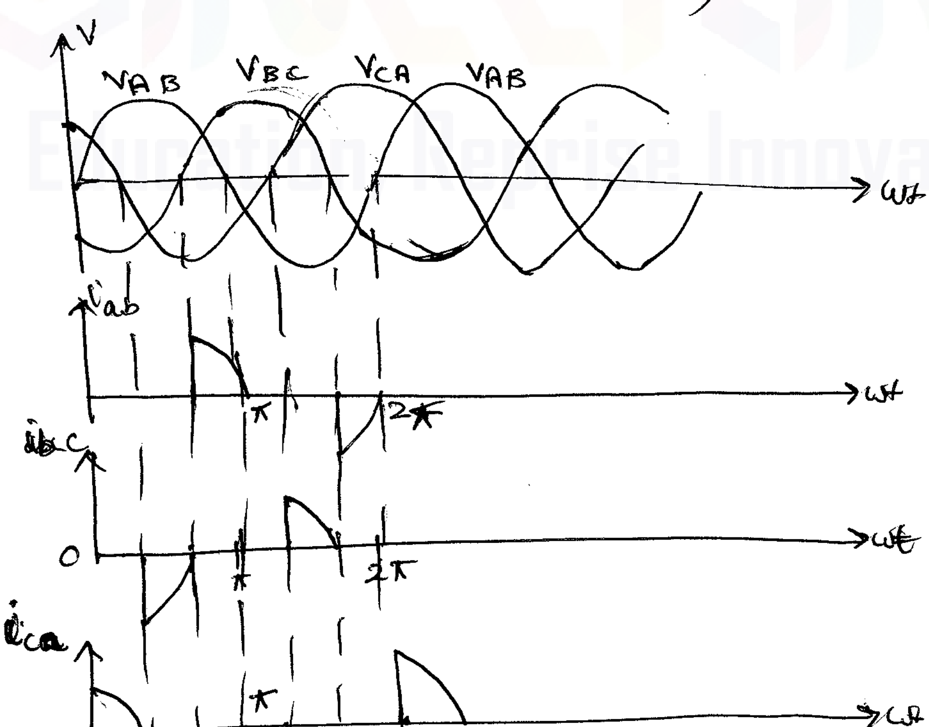
The load is connected in delta. The phase cu… in a normal three phase system is only $1/\sqrt{3}$ of line curre… the current rating of thyristors would be less than that if thyristors were placed in the line.



$$V_{AB} = V_{ab} = \sqrt{2}\,V_s \sin\omega t$$

$$V_{BC} = V_{bc} = \sqrt{2}\,V_s \sin\left(\omega t - 2\pi/3\right)$$

$$V_{CA} = V_{ca} = \sqrt{2}\,V_s \sin\left(\omega t - 4\pi/3\right)$$



for resistive load, the rms o/p phase voltage

$$V_0 = \left[\frac{1}{2\pi}\int_{\alpha}^{2\pi} V_{ab}^2 \, d(\omega t)\right]^{1/2} = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi} 2 V_s^2 \sin \omega t \, d(\omega t)\right]^{1/2}$$

$$= V_s \left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

Maximum o/p voltage obtained when $\alpha = 0$, for $0 \leq \alpha$

The line current $i_a = i_{ab} - i_{ca}$

$i_b = i_{bc} - i_{ab}$

$i_c = i_{ca} - i_{bc}$

The line current depends on the delay angle and may discontinuous. If I_n is the rms value of n^{th} harmonic component of phase current, rms value of phase curren

$$I_{ab} = \left(I_1^2 + I_3^2 + I_5^2 + I_7^2 + \cdots + I_n^2\right)^{1/2}$$

Due to delta connection, triplen harmonic compo of phase current would flow around delta and does appear in line because of the zero sequence harmo are in phase in all three phases of load.

The rms value of line current

$$I_a = \sqrt{3}\left(I_1^2 + I_5^2 + I_7^2 + I_{11}^2 + \cdots\right.$$

Cycloconverters

A device which converts input power of one frequ
to output power at a different frequency with one sta
conversion is called cycloconverter. It is a one stage
frequency changer.

Cycloconverter are of two types (i) Step up cycloconvert
(ii) Step down cycloconve

Step down cycloconverter, $f_o < f_s$ (o/p frequency less than supply frequency)

Step up cycloconverter, $f_o > f_s$ (o/p frequency greater than supply freque

Applications:

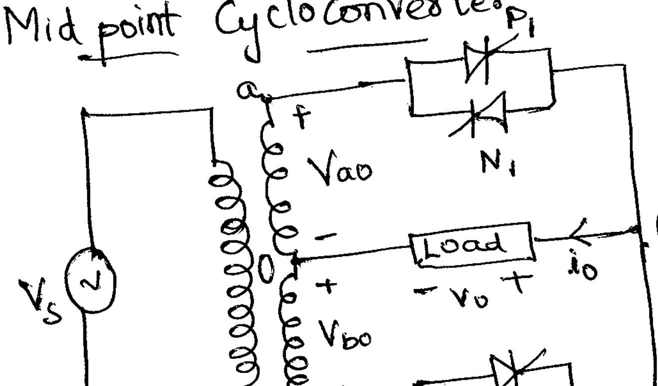
1. Speed control of high power ac drives
2. Induction heating
3. static VAR generation
4. For converting variable speed alternator voltage to constant frequency output voltage for us as power supply in air craft or shift boards

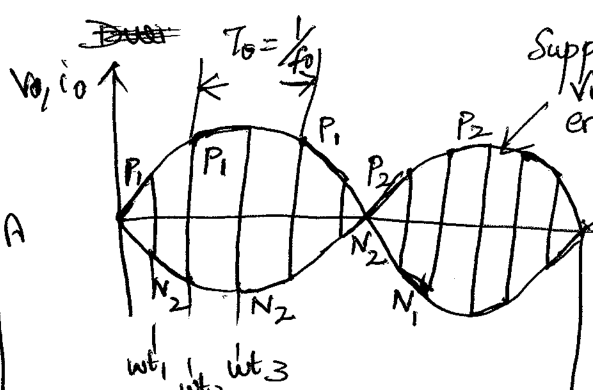
Principle of Cycloconverter operation:

1. Single phase to Single phase Step up cycloconverte

Step up cycloconverter requires forced comm
Step up cycloconverter discussed for midpoint and brid
type converter

Mid point Cycloconverter

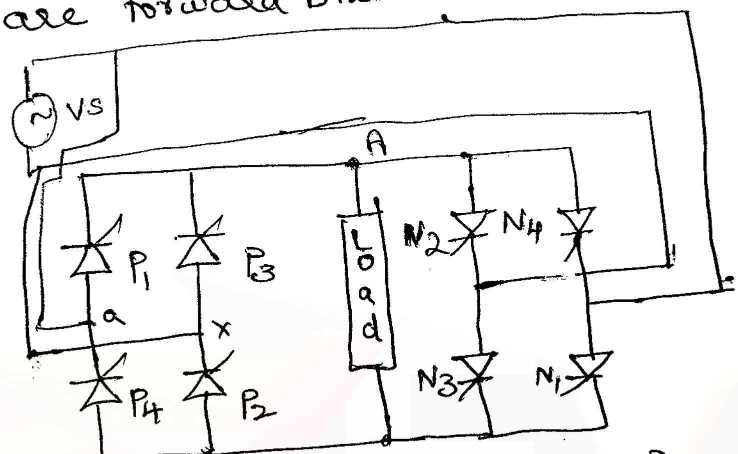




* P_1 P_2 for positive group, N_1 N_2 for negative group. Lo
is connected between secondary winding mid point O
and terminal A.
* During +ve half cycle, terminal a +ve with respect t
* P_1 and N_2 are forward biased from $\omega t = 0$ to π.
* P_1 turned on at $\omega t = 0$ so load voltage is positive wi
terminal A positive and O negative
* load voltage follows positive envelope of supply
* At ωt_1, P_1 is force commutated and N_2 is turned o
So load voltage is negative with terminal O p
and A negative.
* The load or output voltage traces negative enve
of supply voltage.
* At ωt_2, N_2 is force commutated and P_1 is tur
* After $\omega t = \pi$, terminal b is +ve with respect t
* P_2 N_1 are forward biased from $\omega t = \pi$ to 2π.
* At $\omega t = \pi$, N_2 is force commutated and P_2 is tur
* At $\omega t = \frac{1}{2f_s} + \frac{1}{2f_o}$, P_2 is force commutated and N_1
turned on.
* In this way P_1 N_2 for ~~+ve~~ first half cycle and P_2 N_1 f
second half cycle.
* The output frequency higher than supply freque
* $f_o = 6 F_s$.

Bridge Type Cycloconverter

It consists of eigher thyristors, P_1 to P_4 for pos
group and N_1 to N_4 for negative group.
When a is positive with respect to x, P_1, P_2 and $N_1 N$
are forward biased from $\omega t = 0$ to $\omega t = \pi$.



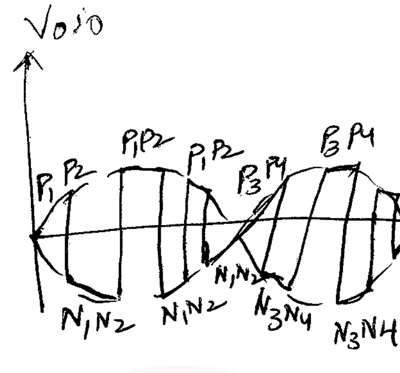


Figure-2

When $P_1 P_2$ are turned on at $\omega t = 0$, load voltage is positi
with respect to x. and terminal positive A with respect to
At ωt_1, $P_1 P_2$ is force commutated and $N_1 N_2$ is turned on.
Load voltage is negative with terminal O positive
with respect to A. load voltage follows negative envelope o
supply voltage.

At $\omega t = \pi$, $P_3 P_4$ and $N_3 N_4$ are forward biased and can
be turned on and forced commutated from $\omega t = \pi$ to 2
A high frequency turning on and force commutation of
pairs $P_1 P_2$, $N_1 N_2$ and $P_3 P_4$, $N_3 N_4$ gives a carrier freq
modulated output voltage across load terminals.

Single phase to Single phase Step Down Cycloconv

This does not require forced commutation
It requires phase controlled converters. These converters
... provided by ac supp

Mid point cycloconverter step Down

(a) Dis continuous load Current:

~~Re~~fer figure 1 for mid point cycloconverter.

when a is positive with respect to O, P_1 is triggered

$\omega t = \alpha$. i_0 starts building up in the positive direction

from A to O. Load current becomes zero at $\omega t = \beta >$

but less than $\pi + \alpha$.

After half cycle b is +ve w.r.t to O. P_2 is triggered

$\pi + \alpha$. load current is positive from A to O and bui

up from zero. At $\omega t = \pi + \beta$ i_0 decays to zero, P_2

naturally commutated.

At $2\pi + \alpha$ P_1 is turned on.

After four positive half cycle N_2 is gated at $4\pi +$

when O is positive with respect to b.

load current direction is reversed. N_2 is triggered

current builds up in negative direction.

In next half cycle when ~~A~~ O is positive w.r.t to

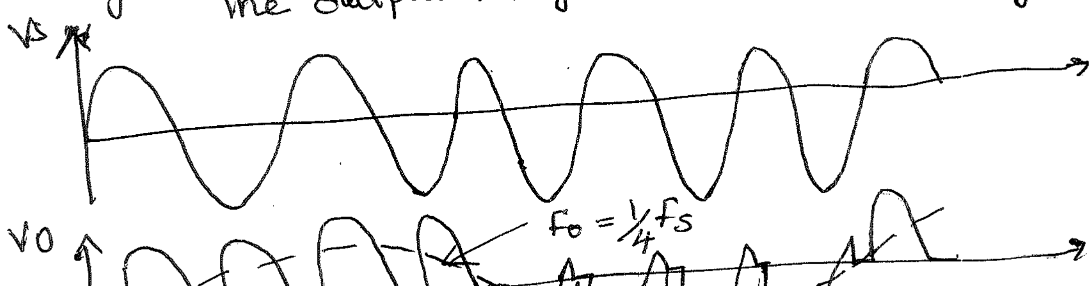
but before N_1 is fired i_0 decays to zero, N_2 is turne

At $5\pi + \alpha$, N_1 is gated i_0 ~~decay~~ builds up from

before the next thyristor N_2 is gated. In this wa

four negative half cycles of load voltage and curre

The output voltage and current for frequency $f_0 =$



Continuous load current

Refer figure 1. P_1 is triggered at $\omega t = \alpha$ positive o/p voltage appears across the load and load current starts building up.

$\omega t = \pi$, $V_0 = 0$. P_1 is R.B. As load current is continu-

P_2 is triggered in sequence at $\pi + \alpha$, a reverse voltage appears across P_1 and turned off by Natural Commutation.

When P_1 is commutated load current has to built up value equal to RR.

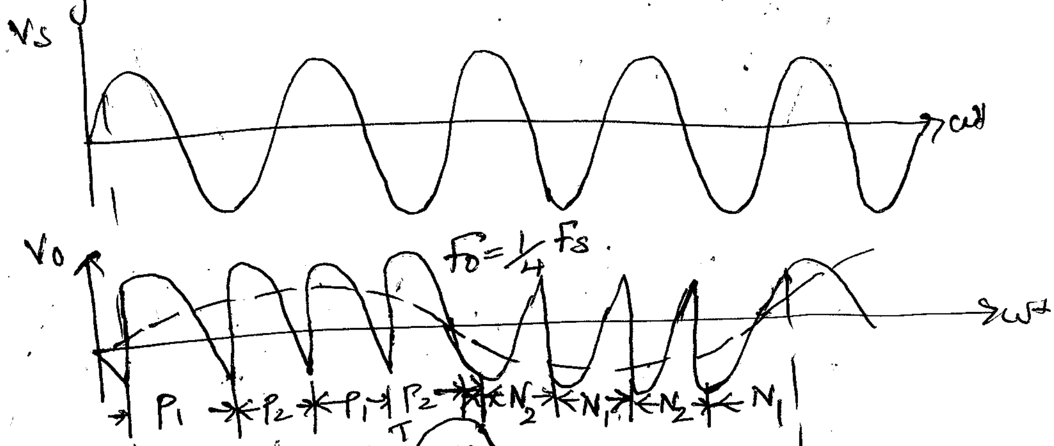
when P_2 turned on $\pi + \alpha$, output voltage again posi- load current still builds up.

At $2\pi + \alpha$. P_1 is turned on P_2 is turned off by natural comm- the load current still builds up

At the end of four positive half cycle the load current

when N_2 is now triggered after P_2 load is subjected to negative voltage cycle and load current i_0 decreases from positive RU to negative AB.

when N_2 is commutated N_1 is gated at $(5\pi + \alpha)$. load current i_0 becomes more negative AB at $6\pi + \alpha$, four negative half cycles of output voltage, load current increas- in the negative direction.



The positive group of voltage and current constitute fo[ur] pulses. and negative group ... Constitute Four Cycles. o/p frequency $f_o = \frac{1}{4} f_s$

<u>Three phase Half wave cycloconverter:</u>

The objective is to consider how single pha[se] low frequency output voltage is fabricated from the seg[ments] of 3-phase input voltage waveform.

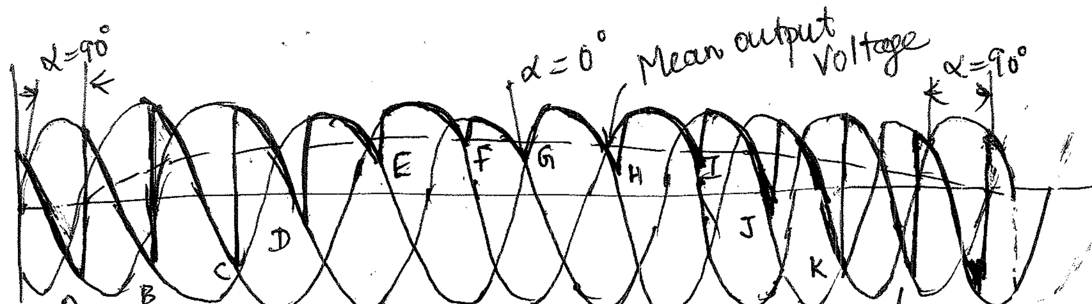
<u>Three phase to Single phase cycloconverters:</u>

The basic principle is to vary progressivel[y] the firing angle of the three thyristors of a 3-phase Ha[lf] wave circuit. The firing angle at A to 90°, B firing ang[le] somewhat less than 90°, C is still further reduced tha[n] is at B and so on. The same way delay in firing angle introduced at C, D, E, F and G. At G the firing angle is and the mean output voltage $V_o = V_{do} \cos\alpha$ is maximum

At A mean o/p voltage is zero $\alpha = 90°$,

At M mean o/p voltage is zero $\alpha = 90°$.

The single phase o/p voltage fabricated from input voltage is shown by thick curve.

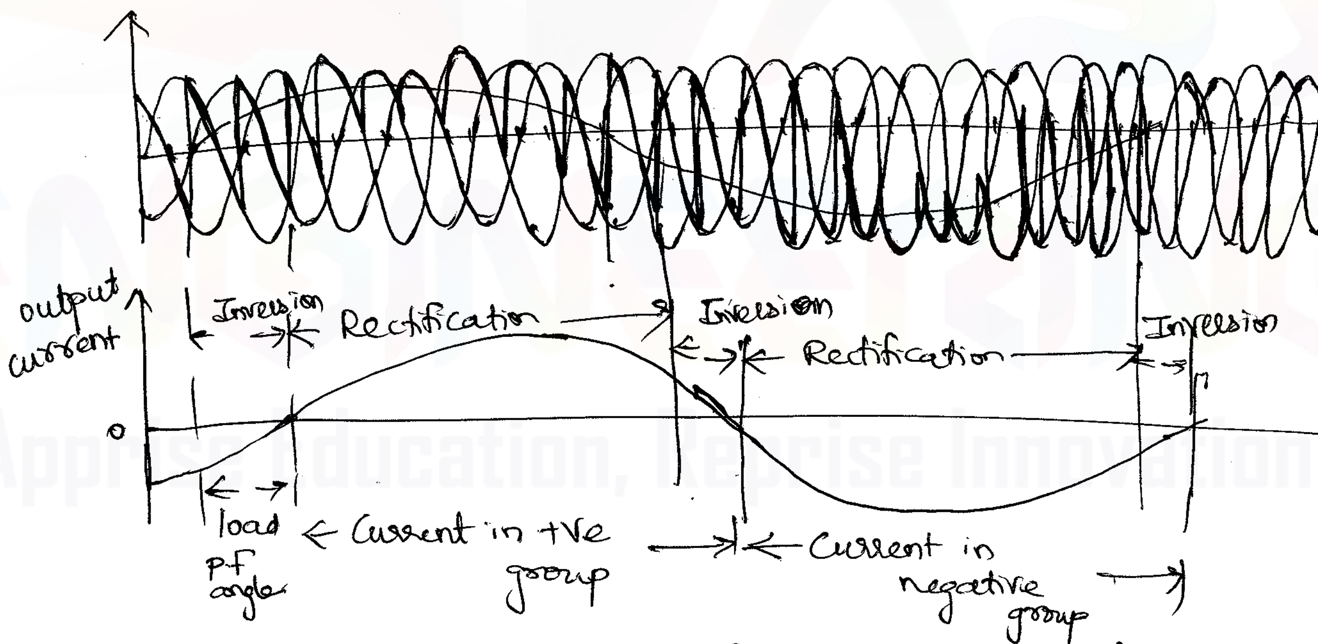


* fabricated output voltage ...
Fundamental frequency output voltage plus several other haemonic components.

* Load inductance filter the high frequency unwanted haemonics.

* For one half cycle of fundamental frequency output voltage there are eight half cycles of supply frequency voltage. O/p frequency $f_o = \frac{1}{8} f_s$.

* For obtaining one cycle of low frequency output voltage the firing angle varied from 90° to 0° to 90° +ve half cycle. and from 90° to 180° to 90° for negative half cycle.



Voltage and current waveforms of 3phase Half wave cycloconverter

The low frequency output voltage can be fabricated from the segments of 3phase input voltage waveform by the use of phase controlled converters. The cycloconverter ...

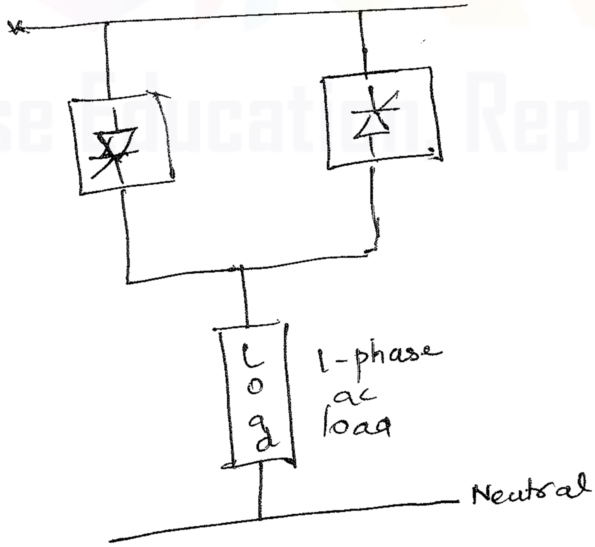
* For allowing flow of current in both the dire
during one complete cycle of load current, two three ph
half wave converters must be connected in ~~para~~
antiparallel.

* The converter permits the flow of current during posit
half cycle of low frequency output current is called
positive converter group

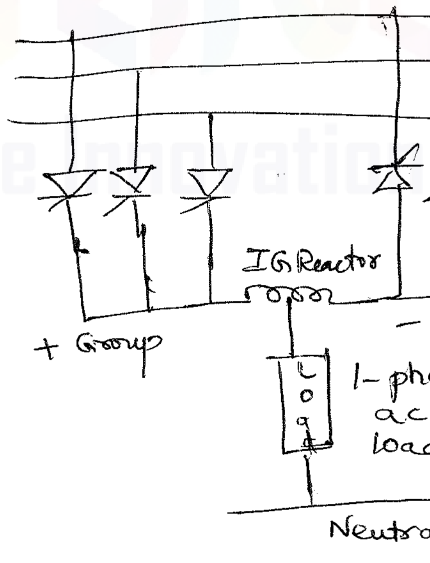
* The converter that permits the flow of current du
negative half cycle of low frequency output cur
is called negative converter group.

From the voltage and current waveforms of 3 phase
Half wave cycloconverter, positive converter acts as a
rectifier when output voltage is positive and as
inverter when o/p voltage negative.

* when o/p current negative, negative converter co
Negative converter acts a rectifier when o/p voltag
negative and as an inverter when o/p voltage posi



Schematic diagram.



Basic circuit
configura

Three phase to single phase cycloconvert

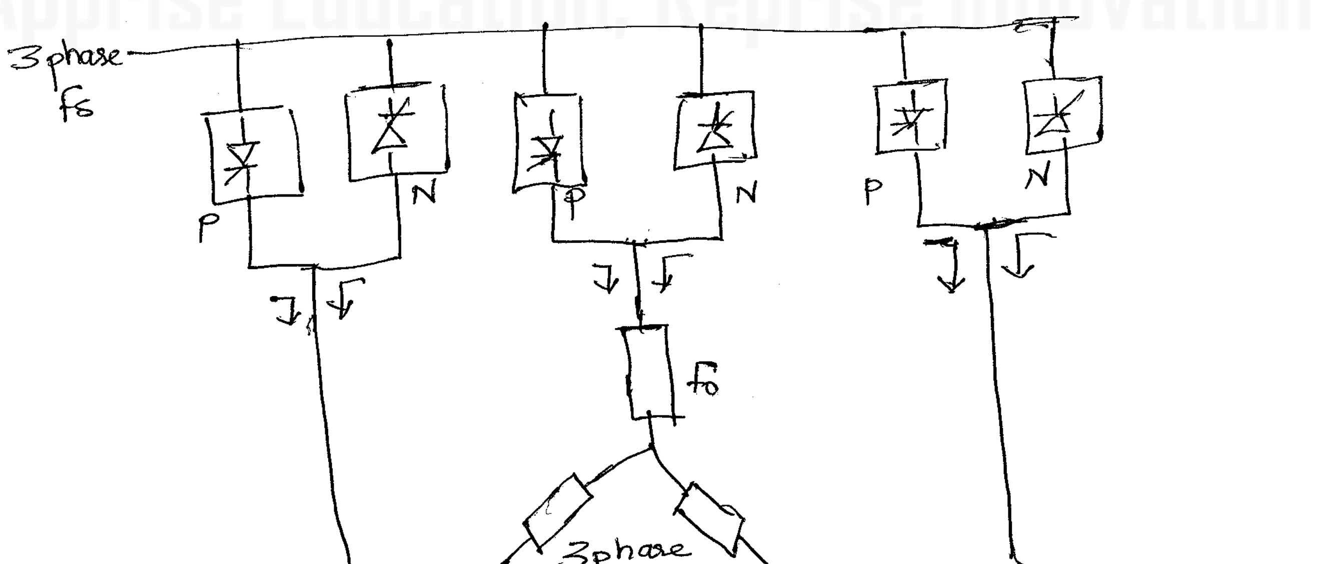
* The output voltage of two converters in the same phase have the same average value, their output voltage waveforms as a function of time are different as a result there will be a net potential difference across two converters.

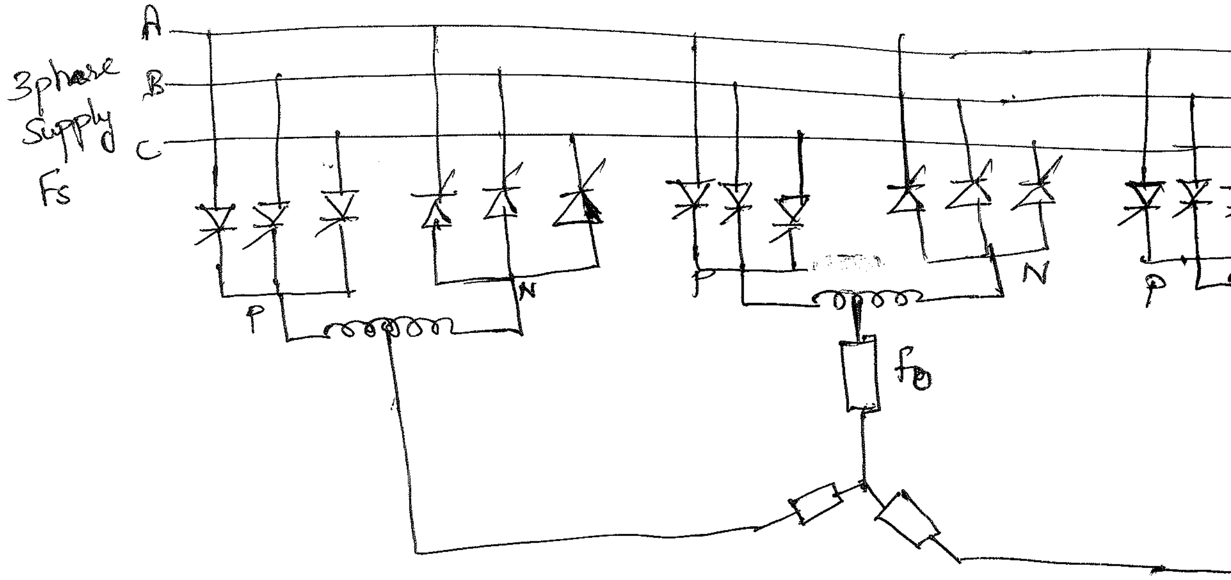
* This net voltage causes a circulating current which can be avoided by removing gating signals from idle converter or by inserting intergroup reactor (IG between positive and negative group converters.

* If $\alpha_p \rightarrow$ firing angle for positive converter
  $\alpha_n \rightarrow$ firing angle for negative converters
  then firing angle should satisfy the condition $\alpha_p + \alpha_n = 1$

Three phase to Three phase cyclo converter

For 3 phase low frequency output three se of phase controlled 3 phase to single phase circuits are interconnected. Each phase of 3 phase output must have a phase displacement of 120°.





Basic Circuit.

The schematic and Basic Circuit arrang[ement] of 3phase to 3 phase cycloconverter is shown a[bove]. 18 thyristors are connected to form 3phase to 3 pha[se] cycloconverter.

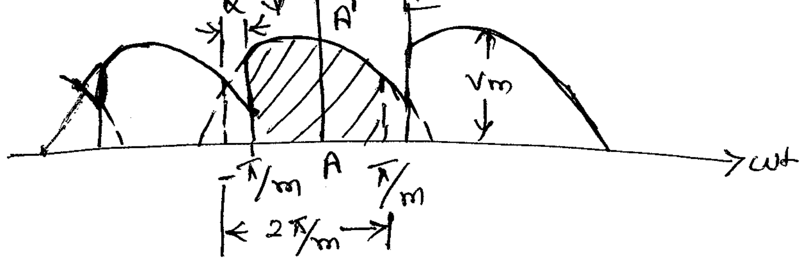
The frequency of output voltage can be va[ried] by changing the sequence of firing of the SCRs. The o/p frequency of cycloconverter is less than the supply frequen[cy].

Output voltage equation for a cycloconverter:-

A cycloconverter is essentially a dual converte[r] which is to be operated to produce an alternating output voltage. Each SCR in a cycloconverter works as phase controlled converter with a varying firing angle.

In 3 phase Half wave converter, each phase conducts for $2\pi/3$ radians of a cycle.

In general m-phase Half wave converter, each



AA' as the peak value of supply voltage.

Instantaneous phase voltage $V = V_m \cos\omega t$

$= \sqrt{2}\, V_{ph} \cos\omega t$

V_{ph} – rms value of per-phase supply voltage.

Conduction takes place from $-\pi/m$ to π/m for $\alpha = 0^\circ$.

for any α the conduction $-\pi/m + \alpha$ to $\pi/m + \alpha$.

Average value of o/p dc voltage V_d, equal to averag[e] height of shaded area.

$$V_d = \frac{m}{2\pi} \int_{-\pi/m+\alpha}^{\pi/m+\alpha} V_m \cos\omega t \, d\omega t = V_m \left[\left(\frac{m}{\pi}\right) \sin\frac{\pi}{m}\right] \cos\alpha$$

For zero firing angle delay

$$V_{do} = V_m \left(\frac{m}{\pi}\right) \sin\frac{\pi}{m} = \sqrt{2}\, V_{ph} \left(\frac{m}{\pi}\right) \sin\frac{\pi}{m}.$$

If V_{or} is the fundamental rms value of per phase output voltage of cycloconverter, the peak o/p voltage for zero firing angle is

$$\sqrt{2}\, V_{or} = V_{do} = \sqrt{2}\, V_{ph} \left(\frac{m}{\pi}\right) \sin\pi/m$$

$$V_{or} = V_{ph} \left(\frac{m}{\pi}\right) \sin\pi/m$$

α_p of positive group cannot be zero, since $\alpha_n = 180 -$

$= 180^\circ$

negative grou[p]

Inverter firing angle never equal to 180° because of commutation overlap and thyristor turn off time.

firing angle of positive group can never be zero but have some finite value. The minimum value of firing for positive group be α_{mn}.

~~$V_{d\,mx}$ cos~~

$$V_{d\,mx} = V_{do} \cos \alpha_{mn} = r\, V_{do}$$

$r = \cos \alpha_{mn}$ is called voltage reduc[tion] factor

Fundamental rms phase value of output voltage [of] cycloconverter

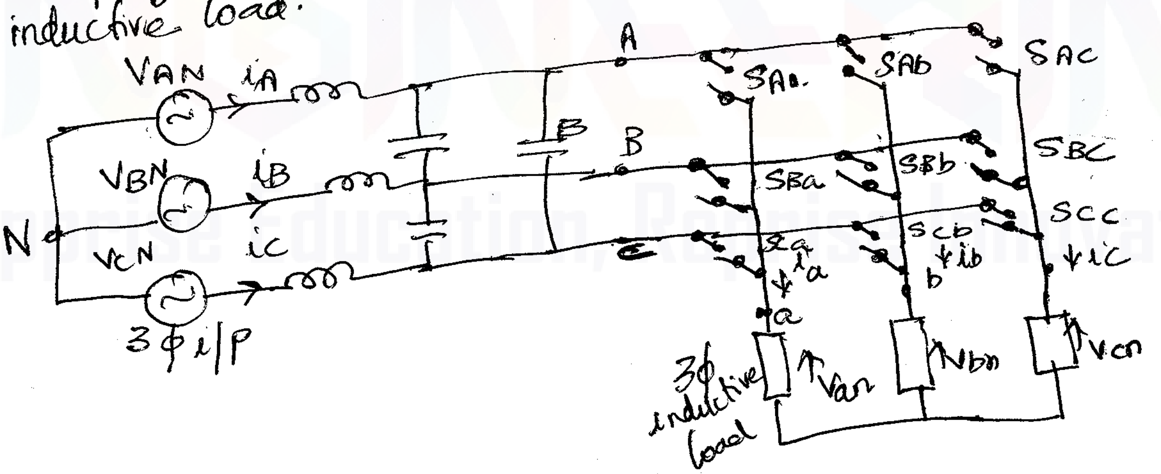
$$V_{or} = r \left[V_{ph} \left(\frac{m}{\pi}\right) \sin\left(\frac{\pi}{m}\right) \right]$$

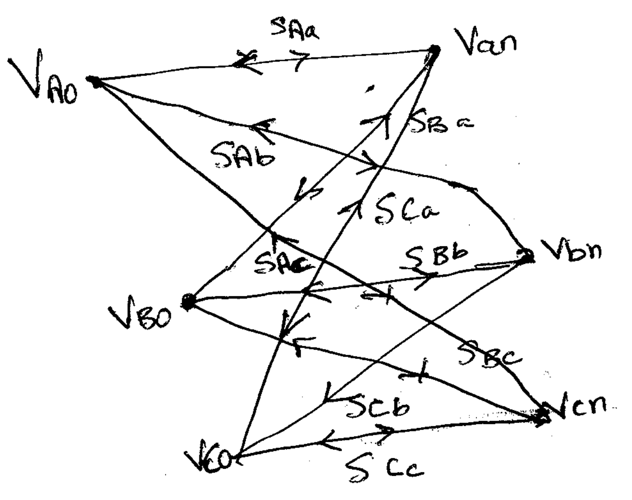
α_{mn} is greater than zero, r is always less [than] unity.

Matrix Converter:-

* Matrix Converter uses bidirectional fully controlled switches for direct conversion from ac to ac.
* Single stage converter that requires only nine switches for three phase to three phase conversion.
* Alternative to the double sided PWM voltage source rectifier inverter.
* The nine bidirectional switches are so arranged that any of three input phase could be connected to any o/p phase through the switching matrix symbol. Thus the voltage at any i/p terminal may be made to appear at any o/p terminal or terminals whereas the current in any phase of load may be drawn from any phase or phases of the i/p supply. An ac input LC filter is normally used to eliminate harmonic currents in the i/p and load is sufficiently inductive to maintain continuity of o/p currents.

Matrix is due to the fact that it uses exactly one switch for each of the possible connections between the i/p and output. The switches should be controlled in such a way that only one of the three switches connected to an o/p phase must be closed to prevent short circuiting of the supply lines or interrupting the load current flow in an inductive load.





27 switch combinations are allowed to produce the o/p line voltages and i/p phase currents.

The matrix converter can be connected at any i/p phase (A, B and C) to any o/p phase (a, b & c) at any instant. When connected the voltages V_{an}, V_{bn}, V_{cn} at the o/p terminals are related to the i/p voltages V_{AN}, V_{BN}, V_{CN}

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix}$$

For a balanced linear Y-connected load at the o/p the i/p phase current are related to the o/p phase currents by

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{AC} \\ S_{Ba} & S_{Bb} & S_{BC} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix}^T \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

The maximum peak to peak of voltage cannot be greater than the minimum voltage difference between two phases of the input. The maximum voltage transfer ratio is 0.866 ... must have ... The control methods for matrix converter ... control of o/p voltage and o/p ... ability for independent control of ... Three types of methods are commonly used.

(i) Venturini method based on a mathematical approach of transfer function analysis

(2) PWM method (3) Space vector modulation.

Advantages of matrix converter:

(1) Inherent bidirectional power flow
(2) Sinusoidal i/p - o/p waveforms with moderate switching ...
(3) Possibility of compact design due to absence of dc link reactive components
(4) Controllable i/p P.F independent of o/p load current.

Applications:

(i) Non availability of bilateral fully controlled monolithic switches capable of high frequency operation.
(ii) Complex control law implementation.
(iii) Intrinsic limitation of o/p - i/p voltage ratio
(iv) Commutation and protection of switches.

Unit - II

Phase Controlled Converters

Industries uses Controllable DC power.

Examples are

(1) Steel rolling mills, paper mills, printing press, & Textile mills

2) Traction System working on DC

3) Magnet power supplies

4) Electrochemical and Electrometallurgical process

5) High voltage DC Transmission.

Phase controlled ac-dc converters employing thyristors are used for changing constant ac i/p voltage to Controlled dc o/p voltage.

SCR and Diodes are ideal switches which means that (i) there is no voltage drop

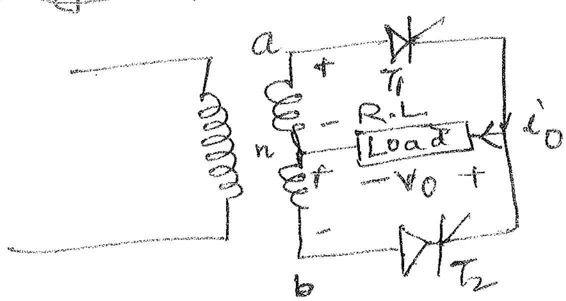
(ii) No reverse Current under reverse voltage

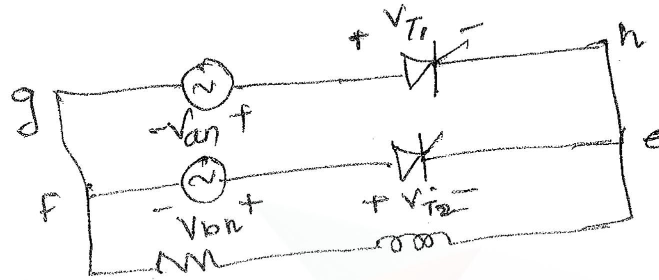
(iii) Holding Current is Zero.

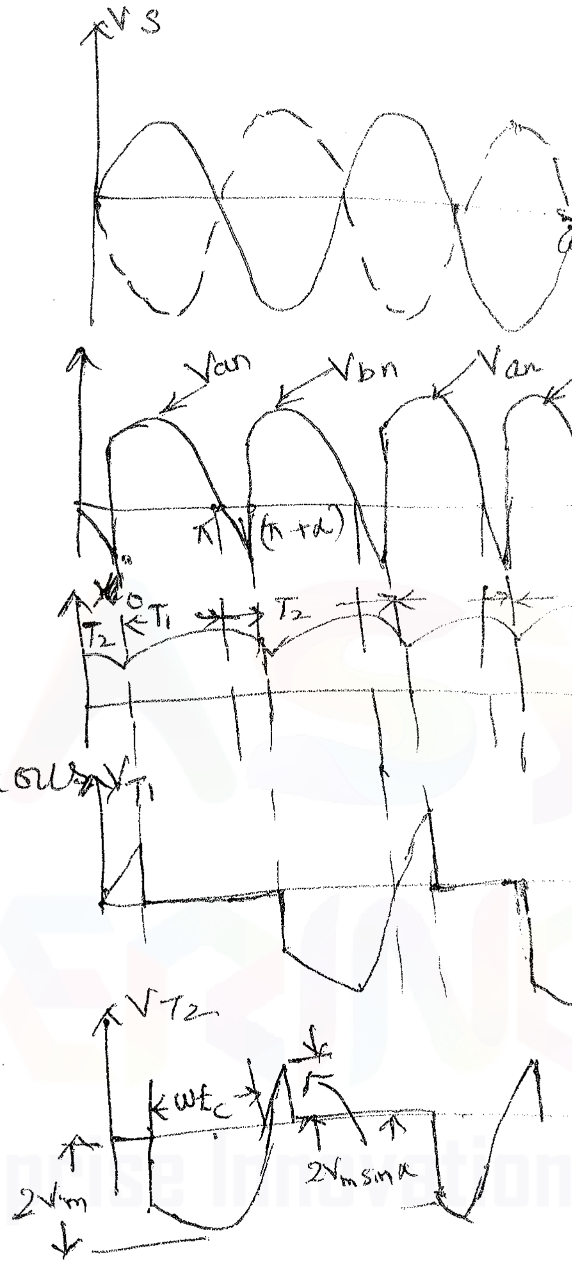
Full wave Controlled converters

- Rectifier
  - Number of Supply
    - 1φ
    - 3φ
  - Load current pulse per cycle of Source voltage
    - 1φ Halfwave or one pulse Converter
    - 1φ Full wave or 2 pulse Converter Bridge Converter
    - 3φ Six pulse

Single phase full wave Mid point converter







Terminal a +ve w.r.t n,

Terminal n positive w.r.t to b

$V_{an} = V_{nb}$ or $V_{an} = -V_{bn}$

Load or O/p current is continuous

Turns ratio unity.

T_1 and T_2 are forward biased during +ve and -ve half cycle.
If T_2 is already conducting. After $\omega t = 0$, V_{an} = +ve, T_1 is forward biased and when triggered at delay angle α, T_1 gets turned on..

At α, supply voltage $2V_m \sin\alpha$ reverse biases T_2. So SCR is turned off. T_1 is the incoming thyristor and T_2 the outgoing thyristor. When the incoming SCR is triggered, ac supply voltage reverse bias across the outgoing thyristor and turns it off. The process of SCR turn off by natural reversal of ac supply voltage is called natural or line commutation.

$$V_{an} = V_m \sin\omega t$$
$$V_{bn} = -V_{nb} = V_m \sin\omega t$$
$$V_{ab} = V_{an} + V_{nb} = 2V_m \sin\omega t$$

At $\omega t = \alpha$, T_1 is triggered. T_2 is reverse voltage $V_{ab} = 2V_m \sin\alpha$.
The magnitude of T_2 can be obtained by KVL loop efghe.

$$V_{T2} - V_{bn} + V_{T1} = 0$$
$$V_{T2} = V_{bn} - V_{an} + V_{T1}$$

when $V_{T1} = 0$, Voltage across T_2, $\omega t = \alpha$,

$$V_{T2} = -V_m \sin\alpha - V_m \sin\alpha = -2V_m \sin\alpha$$

$\omega t = \alpha$, T_2 is turned off and remains reverse biased from $\omega t = \alpha$ to π,
Turn off time is provided by $t_c = \frac{\pi - \alpha}{\omega}$

T_1 is turned off at $\omega t = \pi + \alpha$, T_1 is reverse biased from $\pi + \alpha$ to 2π.
$$t_c = \frac{2\pi - (\pi + \alpha)}{\omega} = \frac{\pi - \alpha}{\omega}$$

Average value of o/p voltage $V_0 = \frac{1}{\pi}\int_{\alpha}^{\alpha+\pi} V_m \sin\omega t \, d\omega t$

$$= \frac{2V_m}{\pi}\cos\alpha.$$

The following observation

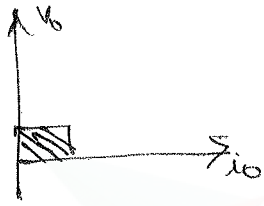
(i) Commutation of an SCR is desired, it must be R.B and incoming SCR must be forward biased
(ii) When incoming SCR is gated, current is transferred from outgoing SCR to incoming SCR
(iii) Circuit turn off time is greater than SCR turn off time.

phase Controlled Converters

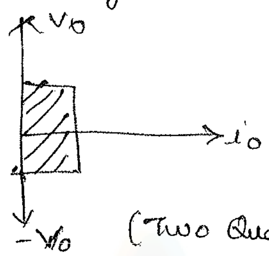
Uncontrolled Converters
* Uses diodes and level of dc o/p voltage cannot be controlled.

half controlled Converters or Semiconverter
Uses mixtured diodes & thyristors limited control over the level of dc o/p Voltage.

fully Controlled Converters or full Converter.
Uses thyristor for wider control over the level of o/p volta[ge]



One quadrant converter



(Two Quadrant converter)

A semiconverter is one quadrant converter which has one polari[ty] of dc o/p voltage and current.

A two quadrant converter is one in which voltage polarity can reverse but current direction cannot reverse because of the unidirectional nature of thyristors.

Single phase Semiconverter:- or Single phase Half Controlled bridge

Two thyristors and three diodes; with T_1 and T_2, two diodes are D_1, D_2, the third diode connected across load is free wheeling diode FD. The load is of RLE types.

$\omega t = 0$, T_1 is forward biased when $V_m \sin\omega t$ exceeds E.

T_1 is fired at angle α. $V_m \sin\alpha > E$.

T_1 on, load gets connected to source, $V_0 = V_s$.

$\omega t = \pi$, V_0 tends to reverse as the ac source voltage changes polarity. when V_0 tends to reverse, FD is forward bia[sed] and starts conducting. i_0 is transfered from T_1, D_1 to FD. when T_1 is R.B at $\omega t = \pi +$, through FD, T_1 is off at $\omega t = \pi +$

The load voltage is zero for $\pi < \omega t < (\pi + \alpha)$.

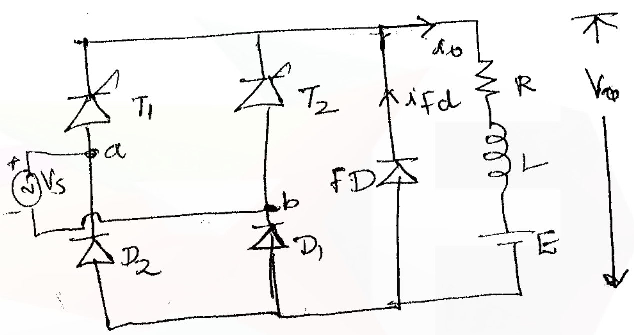
$\omega t = \pi$.. T_2 will be forward biased only when source volt[age] is more than E.

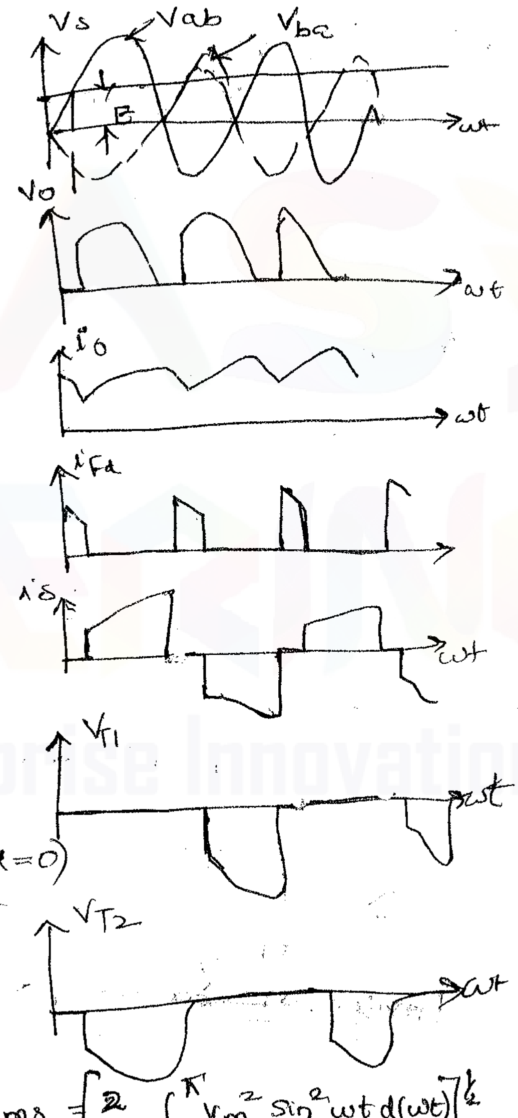
$\omega t = \pi + \alpha$, source voltage exceeds E, T_2 is triggered.

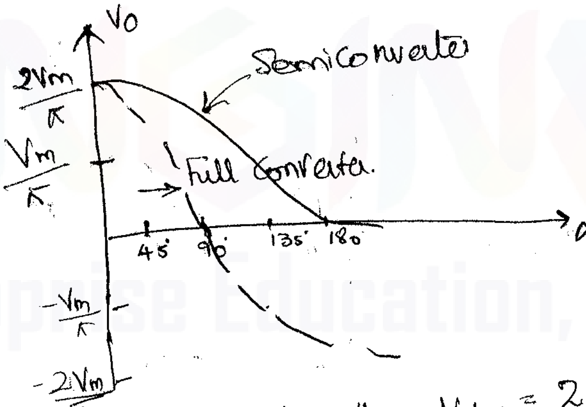
During the interval α to π, T1 and D1 conduct and the source delivers energy to the load circuit. The energy is partially stored in inductance L, partially stored as electric energy in load circuit emf E and partially dissipated as heat in R. During freewheeling period π to (π+α) energy stored in inductance is recovered and is partially dissipated in R and partially stored in load emf E. No energy is added to the energy stored in load during freewheeling period. Fed back to source during

Average o/p voltage $V_0 = \frac{2}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, (d\omega t) = \frac{V_m}{\pi}(1+\cos\alpha) = V_{dc}$

$$t_c = \frac{\pi - \alpha}{\omega}$$







Maximum average o/p voltage $V_{dm} = \frac{2V_m}{\pi}$ $(\alpha = 0)$

$V_n = \frac{V_{dc}}{V_m} = 0.5(1+\cos\alpha)$

$V_{rms} = \left[\frac{2}{2\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\omega t \, d(\omega t)\right]^{\frac{1}{2}}$

$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{\frac{1}{2}}$

Analysis of two pulse converter

Semiconverter:

$V_0 = V_s = R i_0 + L\frac{di_0}{dt} + E \quad \alpha \leq \omega t \leq \pi$

Single phase Semiconverter with Discontinuous ...

SCR, T_1 is triggered at $\omega t = \alpha$, load current builds up from zero, rises to a maximum and then decays to zero at $\beta > \pi$.

$\omega t = \alpha$ to π, $T_1 D_1$ conducts $V_0 = V_s$

$\omega t = \pi$, V_s tends to become negative.

FD is forward biased. from π to β $V_0 = 0$

from β to $\pi+\alpha$, no circuit components conducts so $V_0 = E$.

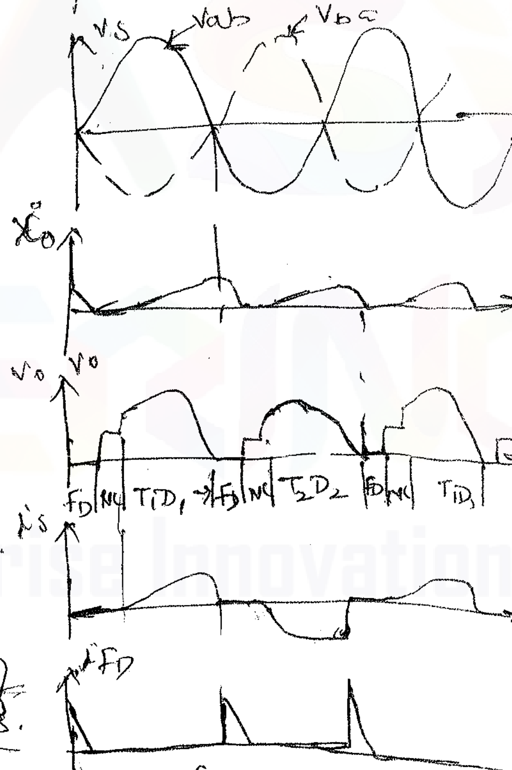
β to $\pi+\alpha$, as load current is zero, load current becomes discontinuous.

T_2 is triggered at $\pi+\alpha$, i_0 builds up.

At 2π, FD is forward biased and starts conducting till $\pi+\beta$

so $V_0 = 0$.

from $\pi+\beta$ to $(2\pi+\alpha)$, no circuit component conducts so $V_0 = E$



$(\pi < \beta < \pi+\alpha)$

(i) conduction period

$\alpha < \omega t < \pi$, $T_1 D_1$ conducts $V_0 = V_s$

$\pi+\alpha < \omega t < 2\pi$, $T_2 D_2$ conducts $V_0 = V_s$

ii) freewheeling period $\pi < \omega t < \beta$.

$i_{fd} = 0$, $V_0 = 0$

$2\pi < \omega t < \pi+\beta$, $V_0 = 0$.

(iii) Idle period $\beta < \omega t < \pi+\alpha$, no circuit component conducts $i_0 = 0$, $V_0 = E$.

Performance measures of two pulse converters.

$$I = \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin \omega t)$$

$$= \sum_{n=1}^{\infty} C_n \sin (n\omega t + \phi_n)$$

$$C_n = \sqrt{a_n^2 + b_n^2} \qquad \phi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right)$$

$$\frac{2}{\pi} \int^{(\pi+\alpha)} \ldots \, d\omega t = \frac{4}{\pi} I_0 \sin\alpha$$

$$C_1 = \sqrt{a_1^2 + b_1^2} = \sqrt{\left(\frac{-4}{\pi} I_d \sin\alpha\right)^2 + \left(\frac{4}{\pi} I_d \cos\alpha\right)^2}$$

$$C_1 = \frac{4 I_d}{\pi}$$

$$I_1 = \frac{C_1}{\sqrt{2}} I_d = \frac{2\sqrt{2} I_d}{\pi}$$

$$\phi_1 = \tan^{-1}\frac{a_1}{b_1} = \tan^{-1}\left[\frac{-\frac{4}{\pi} I_d \sin\alpha}{\frac{4}{\pi} I_d \cos\alpha}\right] = \tan^{-1}(-\tan\alpha) \quad \phi_1 = -\alpha$$

−Ve, Current lags behinds the voltage

(1) Input Displacement Factor = $DSF = \cos\alpha$

(2) Input P.f

$$P.f = \left(\frac{I_1}{I_{rms}}\right)\cos\phi = \left(\frac{\frac{2\sqrt{2} I_d}{\pi}}{I_d}\right)\cos\alpha$$

$$= \frac{2\sqrt{2}}{\pi}\cos\alpha.$$

(3) DC voltage ratio

$$\gamma = \frac{\frac{1}{\pi}\int_{\alpha}^{(\pi+\alpha)} E_m \sin\omega t \, d(\omega t)}{\frac{1}{\pi}\int_0^{\pi} E_m \sin\omega t \, d(\omega t)} = \cos\alpha$$

(4) Input Distortion factor $= \frac{I_1}{I_{rms}} = \frac{2\sqrt{2} I_d}{\pi . I_d} = \frac{2\sqrt{2}}{\pi}$

(5) Input Harmonic factor $I_H = \frac{(I_{rms}^2 - I_1^2)^{1/2}}{I_1}$

$$= \frac{\left[I_d^2 - \left(\frac{2\sqrt{2} I_d}{\pi}\right)^2\right]^{1/2}}{2\sqrt{2} I_d/\pi} = \frac{\left[I_d^2 - \frac{8 I_d^2}{\pi^2}\right]^{1/2}}{2\sqrt{2} I_d/\pi}$$

$$= \frac{\left[\frac{\pi^2 I_d^2 - 8 I_d^2}{\pi^2}\right]^{1/2}}{2\sqrt{2} I_d/\pi} = \left[\frac{\pi^2}{8} - 1\right]^{1/2}$$

(6) Active power ...

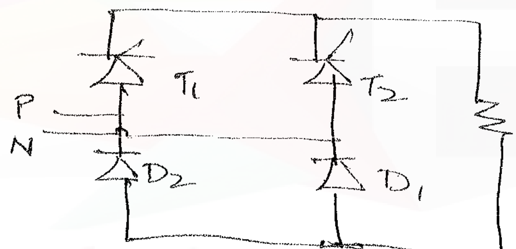
$$K_V = \frac{\sqrt{V_{dc\,rms}^2 - V_{dc}^2}}{V_{dc}} = \frac{\left[\frac{V_m^2}{2} - \left(\frac{2V_m}{\pi}\cos\alpha\right)^2\right]^{1/2}}{\frac{2V_m}{\pi}\cos\alpha}$$

$$= \frac{V_m\left[\frac{1}{2} - \frac{4}{\pi}\cos^2\alpha\right]^{1/2}}{\frac{2V_m\cos\alpha}{\pi}} = \frac{\pi\left[\frac{1}{2} - \frac{4}{\pi^2}\cos^2\alpha\right]}{2\cos\alpha}$$

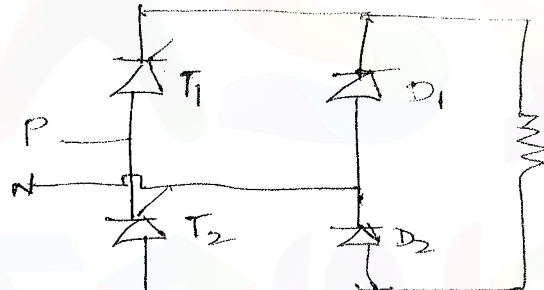
$$= \left[\frac{\pi^2 - 8\cos^2\alpha}{2\cos^2\alpha}\right]^{1/2}$$

$$K_V = \left(\frac{\pi^2}{8\cos^2\alpha} - 1\right)^{1/2}$$

Half Controlled bridge rectifier with Resistive load:- or Semiconverter with Resistive load.



Symmetrical Configuration



Asymmetrical configuration

for symmetrical configuration,
+ve half cycle, T_1 and D_1 are F.B and are in blocking mode when SCR T_1 is triggered at α, the current flow through the path $P - T_1 - R - D_1 - N$. until $\omega t = \pi$.
-ve half cycle, T_2 and D_2 are F.B. and T_2 is triggered at $(\pi+\alpha)$, the current flow through $N - T_2 \cdot R - D_2 - P$. The current is continuous till $\omega t = 2\pi$ and SCR T_2 is turned off.

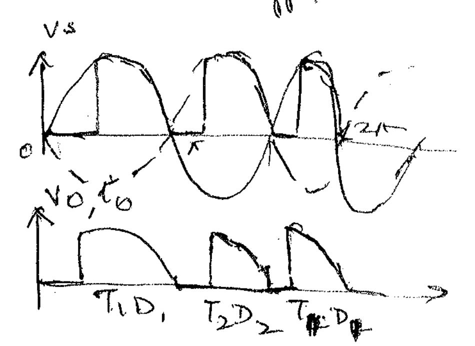
Average load voltage

$$V_0 = \frac{2}{2\pi}\int_\alpha^\pi V_m \sin\omega t\, d\omega t$$

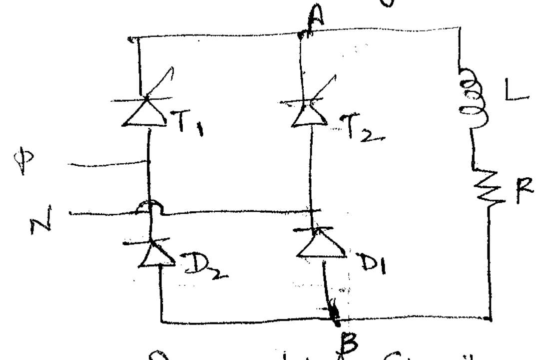
$$= \frac{V_m}{\pi}(1+\cos\alpha)$$

Average load current

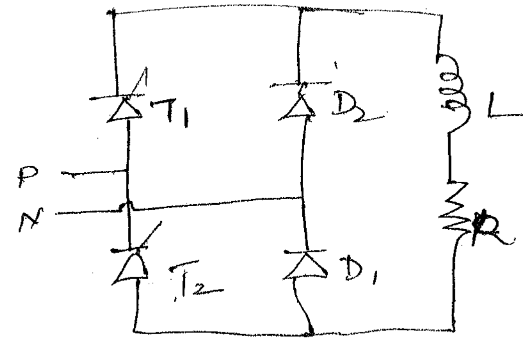
$$I_0 = \frac{V_m}{\pi R}(1+\cos\alpha).$$



Half Controlled bridge rectifier with RL Load:-



Symmetrical Circuit



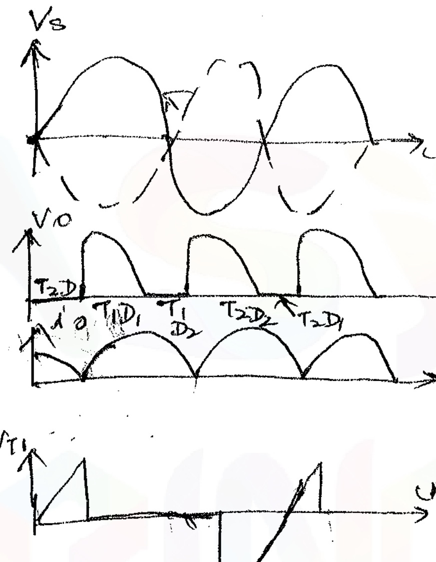
Asymmetry circuit

For symmetry Circuit:-

T_1 is turned on at α for positive half cycle. T_1 and D_1 conducts so load current flows through P $-T_1-A-L-R-B-D_1-N$.

when $\omega t=\pi$, D_2 is F.B and D_1 is conducting. D_2 turns on and load current passes through D_2 and T_1. Supply voltage reverse biases D_1 and turns it off. So load current freewheels through $R-D_2-T_1-$ L during the interval π to $(\pi+\alpha)$

-ve half cycle at $\pi+\alpha$, T_2 is triggered, so the supply voltage R.B T_1 and turns off by line commutation. So load current flows through $T_2 D_2$.



Symmetry circuit

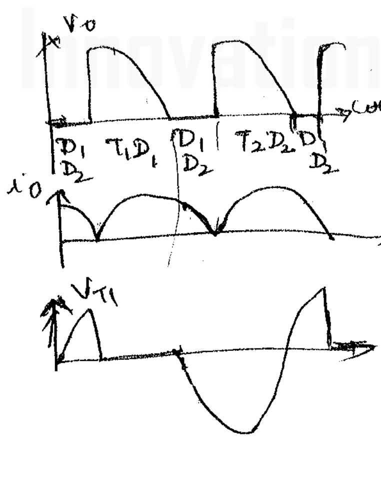
For Asymmetry Circuit:-

+Ve, T_1 and D_1 are F.B. T_1 is turned on at α. So current flows through $P-T_1-A-L-R-D_1-N$.

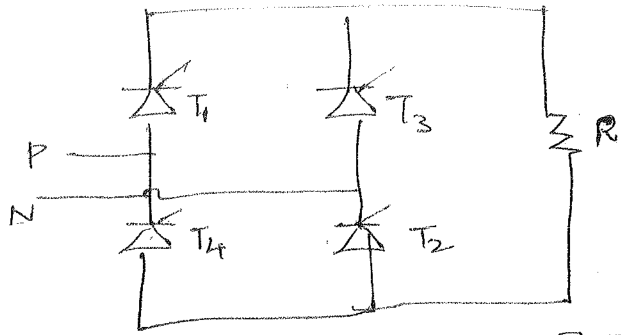
So T_1 & D_1 conducts from α to π.

$|||^{ly}$ T_2 & D_2 conducts from $\pi+\alpha$ to 2π.

Freewheeling action is done by D_1 & D_2 from 0 to α and π to $(\pi+\alpha)$ in each cycle. The conduction period of thyristor and diode are unequal. So it is known as asymmetrical configuration.



Single phase full Converter :- with Resistive Load

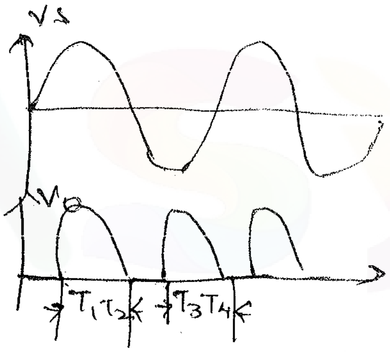


+ve half cycle, T_1 T_2 are F.B and triggered at α. So the current flows through $P - T_1 - R - T_2 - N$.

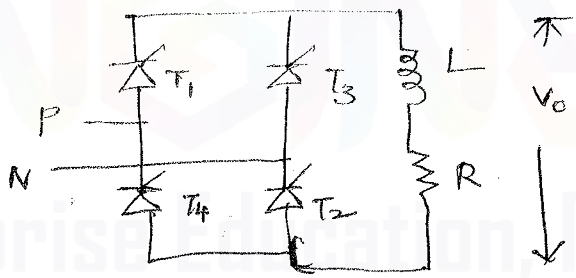
-ve half cycle, T_3 & T_4 are F.B and triggered at $\pi + \alpha$. the current flows through $N - T_3 - R - T_4 - P$. when supply Voltage goes to zero, current goes to zero.

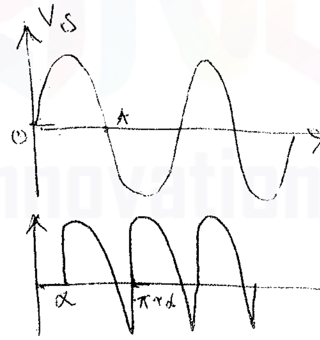
$$V_0 = \frac{2}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left[1 + \cos\alpha\right]$$



1φ full converter with R-L load





T_1 and T_2 are triggered during positive half cycle. Current flows through $P - T_1 - L - R - T_2 - N$.

The load current Id is assumed to be constant.

At instant π, Voltage reverses but because of inductance L, the current is maintained in same direction so T_1 and T_2 are in conduction state.

at $\pi + \alpha$, T_3 and T_4 are fired. The line Voltage reverse biases T_1 and T_2.

So the current flows through $N - T_3 - L - R - T_4 - P$.

Two modes of operation possible with fully controlled single phase circuit

Mode - I: Rectifying mode:

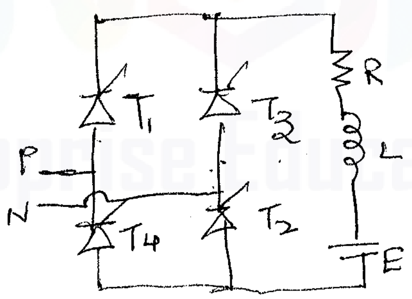
from α to π, V_s and I_s are +ve, so power flows from ac source to π. From π to $\pi+\alpha$, V_s is -ve and I_s +ve, so load returns some of its energy to the supply system. So net power flow is from ac source to load.

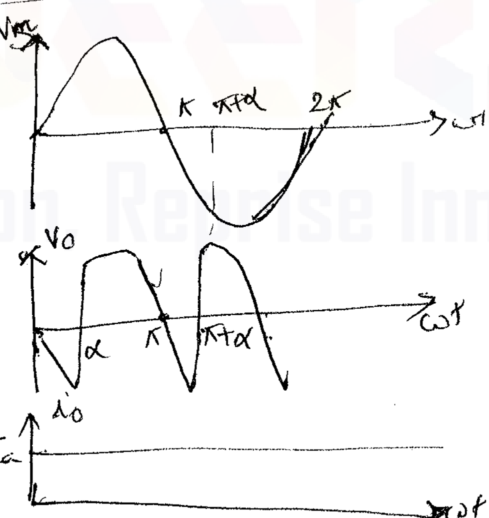
For $\alpha < 90°$, the voltage at dc terminals is +ve, so converter acts as rectifier

Mode 2: Inverting mode:

When the firing angle α is greater than 90°.. the dc voltage becomes negative. or the fundamental component of ac line current waveform lags the voltage by an angle of 135°. Power is delivered from dc side to ac side and the converter is operating as line commutated inverter. for this a source of dc voltage -E whose voltage equals the average dc voltage of converter must be connected at the o/p. This type of operation is used in regenerative breaking mode of dc drives and HVDC transmission.

Single phase full converter with RLE load





$$V_0 = \frac{2}{2\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\Big[\cos\omega t\Big]_{\alpha}^{\pi+\alpha} = \frac{2V_m}{\pi}\cos\alpha$$

The maximum average o/p voltage $V_{dm} = 2V_m/\pi$

$$V_n = \frac{V_{dc}}{V_{dm}} = \cos\alpha.$$

Three phase Controlled Converters

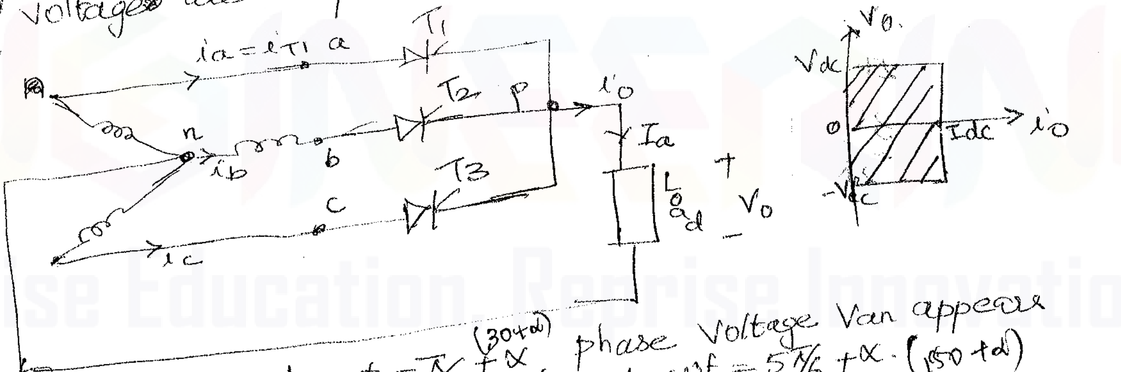
The single phase converter produce a relatively high proportion of ac ripple voltage at its dc terminals. The ripple will be high because of heat producing effect. So a Large value of smoothing reactor is necessary to smoothen the output voltage as well as to reduce the possibility of discontinuous operation. The need for smoothing can be minimized by increasing the number of pulses.

When the number of pulse increases the o/p voltage increases so the ripple content decreases. Three phase is classified as (i) Three pulse converters (ii) Six-pulse converters (iii) Twelve pulse converters.

Three phase half wave converters:

This is called as midpoint configuration.

This converter produce high average o/p voltage and the frequency of ripples on the output voltage is higher compared with that of a single phase converters. The filter requirements for smoothing out the load current and load voltages are simpler.



Thyristor T_1 is fired at $\omega t = \pi/6 + \alpha$ $(30+\alpha)$, phase voltage Van appears across the load until thyristor T_2 is fired at $\omega t = 5\pi/6 + \alpha$ $(150+\alpha)$. When T_2 is fired thyristor T_1 is reverse biased because the line to line voltage $V_{ab} = V_{an} - V_{bn}$ is negative and T_1 is turned off. The phase voltage V_{bn} appears across the load until thyristor T_3 is fired at $\omega t = 3\pi/2 + \alpha$ $(270+\alpha)$. When T_3 is fired, T_2 is turned off and V_{cn} appears across the load until T_1 is fired again at the begining of next cycle. This is a two quadrant converter.

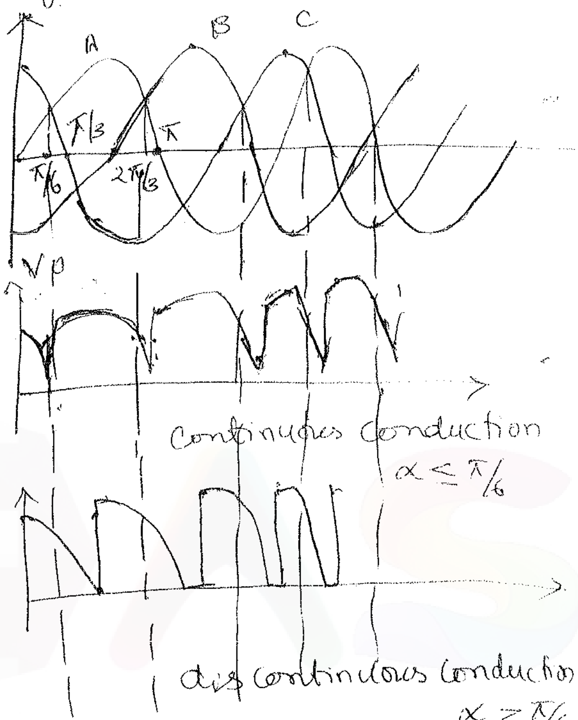
... load there are two modes of conduction ... for $\alpha \leq 30^\circ$

load current is continuous. The maximum value of conduction angle of an SCR is 120°. Therefore for firing angle $\alpha \le 30°$ we have continuous conduction mode of operation.

When $\alpha > 30°$, the conduction angle will be less than 120°. So the o/p voltage and current becomes discontinuous. that is during some time voltage and current remains at zero.

Resistive load

$$V_0 = \frac{1}{2\pi/3} \int_{\pi/6+\alpha}^{5\pi/6+\alpha} V_m \sin\omega t \, d\omega t$$



$$= \frac{3V_m}{2\pi}\Big[-\cos\omega t\Big]_{\pi/6+\alpha}^{5\pi/6+\alpha}$$

$$= \frac{3V_m}{2\pi}\left[-\cos\left(\frac{5\pi}{6}+\alpha\right) + \cos\left(\frac{\pi}{6}+\alpha\right)\right]$$

$$\cos C - \cos D = -2\sin\frac{C+D}{2}\sin\frac{C-D}{2}$$

$$= \frac{3V_m}{2\pi}\left[-2\sin\frac{\pi/6+\alpha+5\pi/6+\alpha}{2}\;\sin\frac{\pi/6+\alpha-5\pi/6-\alpha}{2}\right]$$

$$= \frac{3V_m}{2\pi}\left[2\sin\left(\frac{\pi+2\alpha}{2}\right)\sin\frac{4\pi/6}{2}\right]$$

$$= \frac{3V_m}{2\pi}\left[2\sin\left(\frac{\pi}{2}+\alpha\right)\sin\frac{\pi}{3}\right]$$

$$\sin(90+\alpha) = \cos\alpha$$

$$= \frac{3V_m}{2\pi}\left[2\cos\alpha\,\frac{\sqrt{3}}{2}\right]$$

$$\boxed{V_0 = \frac{3V_m\sqrt{3}}{2\pi}\cos\alpha}$$

Load current

$$I_d = \frac{3\sqrt{3}\,V_m\cos\alpha}{2\pi R}$$

(iii) RMS load voltage

$$V_{rms} = \left[\frac{3}{2\pi}\int_{\pi/6+\alpha}^{5\pi/6+\alpha} V_m^2\sin^2\omega t\, d\omega t\right]^{1/2} = \left[\frac{3V_m^2}{2\pi}\int_{\pi/6+\alpha}^{5\pi/6+\alpha}\left(\frac{1-\cos 2\omega t}{2}\right)d\omega t\right]^{1/2}$$

$$\sin C - \sin D = 2\cos\frac{C+D}{2}\ \sin\frac{C-D}{2}$$

$$C = 2\left(\frac{5\pi}{6}+\alpha\right) \qquad D = 2\left(\frac{\pi}{6}+\alpha\right)$$

$$= \frac{-3}{8\pi}\left[2\cos 2\left(\frac{\frac{5\pi}{6}+\alpha+\frac{\pi}{6}+\alpha}{2}\right)\ \sin 2\left(\frac{\frac{5\pi}{6}+\alpha-\frac{\pi}{6}-\alpha}{2}\right)\right]$$

$$= \frac{-3}{8\pi}\left[2\cos 2\left(\frac{\pi+2\alpha}{2}\right)\ \sin 2\left(\frac{4\pi/6}{2}\right)\right]$$

$$= \frac{-3}{8\pi}\left[2\cos 2\left(\frac{\pi}{2}+\alpha\right)\ \sin\frac{2\pi}{3}\right]$$

$$= \left[\frac{-3}{8\pi}\ 2(-\cos 2\alpha)\frac{\sqrt{3}}{2}\right]$$

$$= V_m\left[\frac{3}{4\pi}\left(\frac{4\pi}{6\cdot 2}\right) - \frac{3}{8\pi}\ 2(-\cos 2\alpha)\frac{\sqrt{3}}{2}\right]^{1/2}$$

$$= V_m\left[\frac{1}{2} - \frac{3}{8\pi}\ 2(-\cos 2\alpha)\frac{\sqrt{3}}{2}\right]^{1/2} = V_m\left[\frac{1}{2} + \frac{3\sqrt{3}}{8\pi}\cos 2\alpha\right]^{1/2}$$

(2) Discontinuous conduction mode $\left(\frac{\pi}{6} < \alpha < 150^\circ\right)$

(i) Average load voltage

$$V_{dc} = \frac{1}{2\pi/3}\int_{\pi/6+\alpha}^{\pi} V_m \sin\omega t\, d\omega t = \frac{3V_m}{2\pi}\left[-\cos\omega t\right]_{\pi/6+\alpha}^{\pi}$$

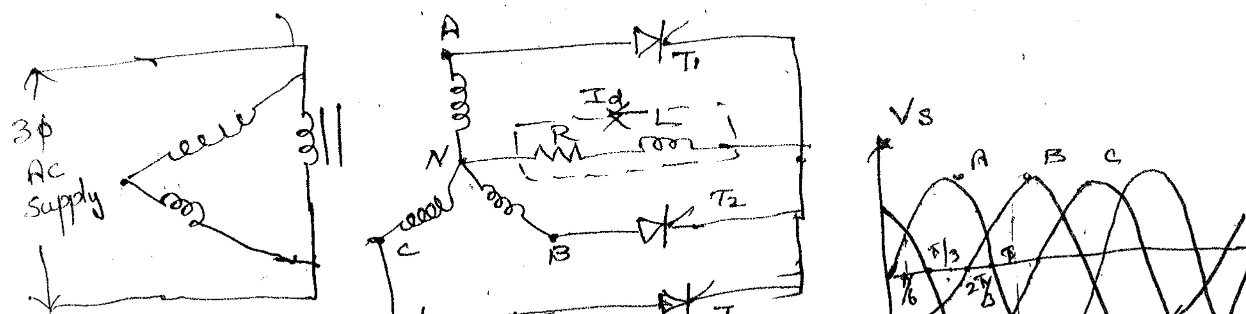
$$= \frac{3V_m}{2\pi}\left[-\cos\pi - \cos\left(\frac{\pi}{6}+\alpha\right)\right] = \frac{3V_m}{2\pi}\left[1+\cos\left(\frac{\pi}{6}+\alpha\right)\right]$$

(ii) $$I_d = \frac{3V_m}{2\pi R}\left[1+\cos\left(\frac{\pi}{6}+\alpha\right)\right]$$

(iii) RMS load voltage: $$V_{rms} = \left[\frac{1}{2\pi/3}\int_{\pi/6+\alpha}^{\pi} V_m^2 \sin^2\omega t\, d\omega t\right]^{1/2}$$

$$= \frac{\sqrt{3}V_m}{2\sqrt{2}}\left[\frac{5\pi-3\alpha}{3\pi} + \frac{\sin\left(2\alpha+\pi/3\right)}{\pi}\right]^{1/2}$$

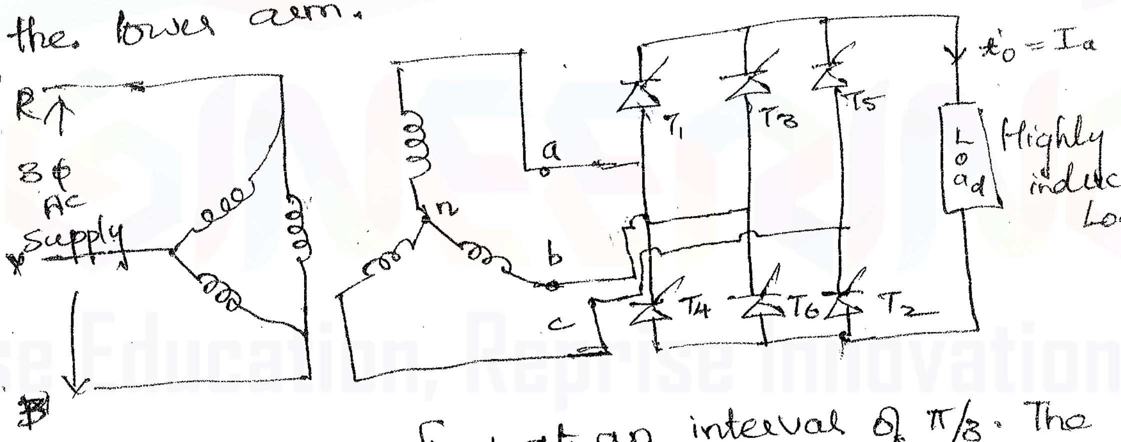
Three phase Half wave Controlled Rectifier with inductive Load (R-L)



3 φ Fully Controlled Bridge Converter

Six pulse converter circuit is obtained by connecting a dc terminal of two 3-pulse converters in parallel. The load is fed via a three phase half wave connection to one of the three supply lines. no neutral being required.

If transformer is used then one winding is connected in delta because the delta connection gives the circulating path for the harmonic current. So third harmonic doesnot appear in line which is an advantage. The circuit consist of positive and negative group of SCRs. The T_1, T_3, T_5 form a positive group and T_4, T_6, T_2 form a negative group. Positive group SCRs are turned on when supply voltages are positive and negative group are turned on when the supply voltages are negative. If one SCR conducts there will be no current flow. So two thyristor must be fired at the same time in to commence current-flow, one of the upper arm and one of the lower arm.



The thyristors are fired at an interval of $\pi/3$. The frequency of o/p ripple voltage is $6f_s$ and the filtering requirement is less than that of half wave converter.

At $\omega t = \pi/6 + \alpha$, T_6 is conducting and T_1 is turned on.

During the interval $(\pi/6 + \alpha) \le \omega t \le (\pi/2 + \alpha)$, T_1 and T_6 conduc and the line to line voltage $V_{ab} = (V_{an} - V_{bn})$ appears across the load.

At $\omega t = \frac{\pi}{2} + \alpha$, T_2 is fired and T_6 is reverse biased. T_6 ... off due to natural commutation. During the interval

The firing sequence is 12, 23, 34, 45, 56 and 61.

If the line to neutral voltages are defined.

$$V_{an} = V_m \sin\omega t$$

$$V_{bn} = V_m \sin(\omega t - 2\pi/3)$$

$$V_{cn} = V_m \sin(\omega t + 2\pi/3)$$

Line to line voltages are

$$V_{ab} = V_{an} - V_{bn} = \sqrt{3}\, V_m \sin(\omega t + \pi/6)$$

$$V_{bc} = V_{bn} - V_{cn} = \sqrt{3}\, V_m \sin(\omega t - \pi/2)$$

$$V_{ca} = V_{cn} - V_{an} = \sqrt{3}\, V_m \sin(\omega t + \pi/2)$$

The average voltage is $\Rightarrow V_0 = \frac{6}{2\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha} V_{ab}\, d\omega t$

$$V_0 = \frac{3}{\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha} V_{ab}\,(d\omega t) = \frac{3}{\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha} \sqrt{3}\, V_m \sin(\omega t + \pi/6)\, d\omega t$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[-\cos(\omega t + \pi/6)\right]_{\pi/6+\alpha}^{\pi/2+\alpha}$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[-\cos\left(\frac{\pi}{2}+\alpha+\pi/6\right) + \cos\left(\pi/6+\alpha+\pi/6\right)\right]$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[\cos(\pi/3+\alpha) - \cos\left(\frac{2\pi}{3}+\alpha\right)\right]$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[-2\sin\left(\frac{\frac{\pi}{3}+\alpha+2\pi/3+\alpha}{2}\right)\sin\left(\frac{\pi/3+\alpha-2\pi/3-\alpha}{2}\right)\right]$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[-2\sin\left(\frac{\frac{3\pi}{3}+2\alpha}{2}\right)\sin\left(\frac{-\pi/3}{2}\right)\right]$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[-2\sin\left(\frac{\pi}{2}+\alpha\right)\sin\left(-\frac{\pi}{6}\right)\right] \qquad \sin(90+\theta) = \cos\theta$$

$$= \frac{3\sqrt{3}V_m}{\pi}\left[2\cos\alpha\,\frac{1}{2}\right]$$

$$\boxed{V_0 = \frac{3\sqrt{3}V_m}{\pi}\cos\alpha}$$

Average o/p voltage for delay angle $\alpha = 0$

$$V_{dm} = \frac{3\sqrt{3}V_m}{\pi}$$

Rms value of o/p voltage

$$V_{orms} = \left[\frac{3}{\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha}\left(\sqrt{3}V_m \sin(\omega t + \pi/6)\right)^2 d\omega t\right]^{1/2}$$

$$= \left[\frac{9V_m^2}{\pi}\int_{\pi/6+\alpha}^{\pi/2+\alpha}\sin^2(\omega t+\pi/6)\, d\omega t\right]^{1/2}$$

$$= \frac{9V_m^2}{\pi}\left[\int_{\pi/6+\alpha}^{\pi/2+\alpha}(1-\cos 2(\omega t+\pi/6))\, d\omega t\right]^{1/2}$$

$$= \frac{9V_m^2}{\pi}\left[\left[\omega t\right]_{\pi/6+\alpha}^{\pi/2+\alpha} - \frac{1}{2}\left[\sin 2(\omega t+\pi/6)\right]_{\pi/6+\alpha}^{\pi/2+\alpha}\right]^{1/2}$$

$$= \frac{9V_m^2}{\pi}\left[\frac{\pi}{2}+\alpha - \frac{\pi}{6} - \alpha\right] - \frac{1}{2}\left[\sin 2\left(\left(\frac{\pi}{2}+\alpha\right)+\pi/6\right) - \sin 2\left(\pi/6+\alpha+\pi/6+\alpha\right)\right]^{1/2}$$

$$= \frac{9V_m^2}{\pi}\left[\frac{\pi}{3} - \frac{1}{2}\left[\sin 2\left(\frac{2\pi}{3}+\alpha\right) - \sin 2\left(\frac{\pi}{3}+2\alpha\right)\right]\right]^{1/2}$$

$$= \frac{9V_m^2}{\pi}\left[\frac{\pi}{3} - \frac{1}{2}\left[2\cos 2\frac{\left(\frac{2\pi}{3}+\alpha+\frac{\pi}{3}+2\alpha\right)}{2}\sin 2\frac{\left(\frac{2\pi}{3}+\alpha - \ldots 2\alpha\right)}{2}\right.\right.$$

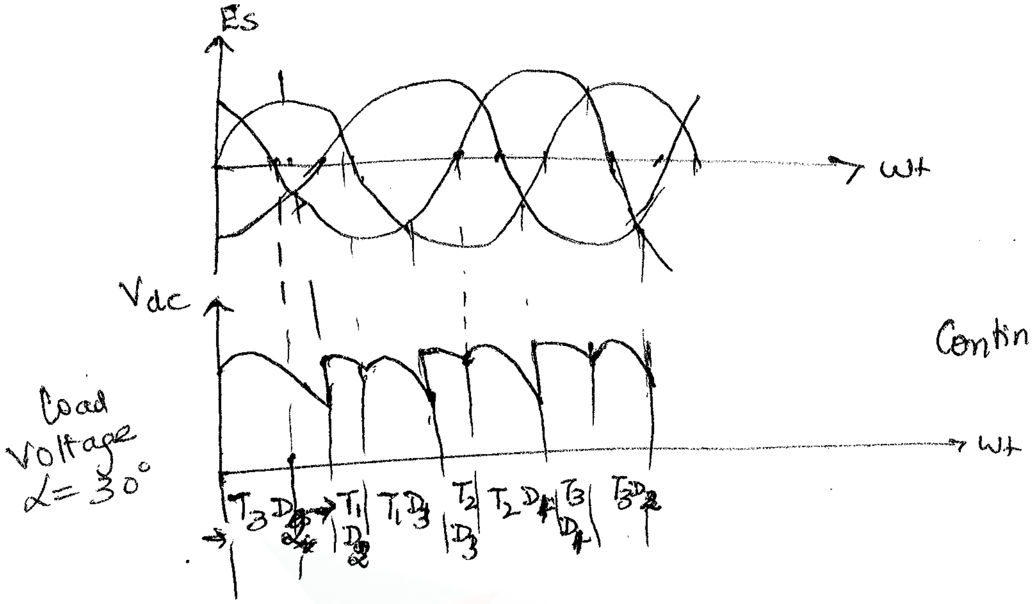
$$= \frac{9V_m^2}{\pi}\left[\frac{\pi}{3} - \frac{1}{2}\left[2\cos 2\frac{(\pi+3\alpha)}{2}\sin 2\frac{\left(\frac{\pi}{3}-\alpha\right)}{2}\right]\right]^{1/2}$$

$$= \frac{9V_m^2}{2\pi}\left[\frac{\pi}{3} - \frac{1}{2}\left[2\cos 2\left(\frac{\pi}{2}+\alpha\right)\sin\left(\frac{\pi}{3}-\alpha\right)\right]\right]^{1/2}$$

$$= \frac{9V_m^2}{2\pi}\left[\frac{\pi}{3} - \frac{1}{2}\left[-2\cos 2\alpha\left[\sin\frac{\pi}{3}\cos\alpha - \cos\frac{\pi}{3}\sin\alpha\right]\right]\right]^{1/2}$$

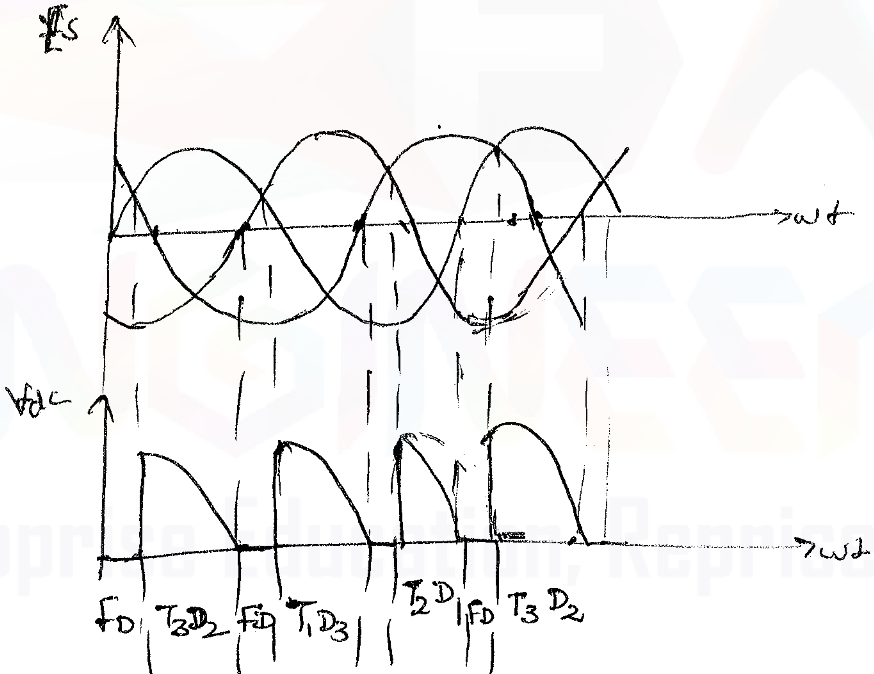
$$= \frac{9V_m^2}{2\pi}\left[\frac{\pi}{3} - \frac{1}{2}\left[-2\cos 2\alpha\left[\frac{\sqrt{3}}{2}\cos\alpha - \frac{1}{2}\sin\alpha\right]\right]\right]^{1/2}$$

$$= \frac{3V_m}{2}\left[\frac{2}{3} + \frac{\sqrt{3}}{\pi}\cos 2\alpha\right]^{1/2} \quad \text{for } 0 \le \alpha \le 180^\circ$$



Continuous Conduction mode

Discontinuous Conduction mode:

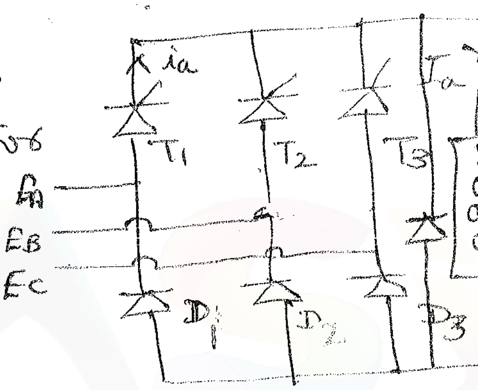


* For $\alpha > 60°$, discontinuous mode takes place. The o/p voltage becomes zero during a part of o/p voltage period because of freewheeling action.
* The freewheeling period is $(\alpha - \pi/3)$.
* The o/p current flows for the period $(\pi - \alpha)$ in each half cycle.

Advantages of six pulse converter with three pulse converter

1. Commutation is made very easier
2. Distortion is reduced due to the reduction in lower ord[er] haemonics
3. Inductance required in series is considerably redu[ced]

Three phase Half controlled bridge converter or Three phase semiconverter



* Three thyristor T_1, T_2, T_3 and Diodes D_1, D_2, D_3 forms a Semiconverter for three phase. Each diodes conducts for 120° period.

Continuous Conduction Mode:

$\alpha < 60°$,

* At instant P thyristor T_1 is triggered with a firing angle. Since A-B has the highest value compared to other phases, thyristor T_1 becomes on.
* Load current flows through A - T_1 - load - D_2 - B
* After (A-B) phase (A-C) has the highest value.
  * The return path shifts from B to phase C,
  * From diode D_2 it changes to D_3.
  * T_1 conducts for 120°
  * The conduction region of all the device is shown
  * The output voltage never goes negative.

Load Voltage

$$V_{dc} = \frac{\sqrt{3}V_m}{2\pi/\ldots} \int^{2\pi/3} \sin\omega t\,(d\omega t) + \int^{2\pi/3+\alpha} \sin\omega t\,(d\omega t)$$

Effect of Source impedance on the performance of Converters

For 1ϕ full wave full bridge circuit, the commutation of SCR takes place instantaneously (ie) as soon as SCR 3 & 4 fire, 1,2 is turned off due to the application of reverse voltage and current will shift to SCR 3,4 from 1,2. This is possible when source has no internal impedance. The effect of source inductance is to delay the commutation of current from one pair of SCR to another.

If the source impedance is resistive, commutation will be complete when the circulating current flowing from the firing of next pair of SCR is equal to load current

for single phase $\rightarrow \frac{V_i}{r_s}$ (circulating current)

$3\phi - \frac{V_a - V_o}{2r_s}$ r_s - source resistance.

Since r_s is initially small, it is assumed that duration of commutation is also very small and can be neglected.

V_s still produces a constant voltage drop $I_o r_s$. this must be subtracted from the average in the dc o/p voltage output voltage.

$$V_o = \frac{2V_m}{\pi}\cos\alpha - I_o r_s \rightarrow 1\phi$$

$$V_o = \frac{3\sqrt{3}V_m}{\pi}\cos\alpha - 2I_o r_s \rightarrow 3\phi.$$

If the source impedance is purely reactive then the commutation period will be μ.

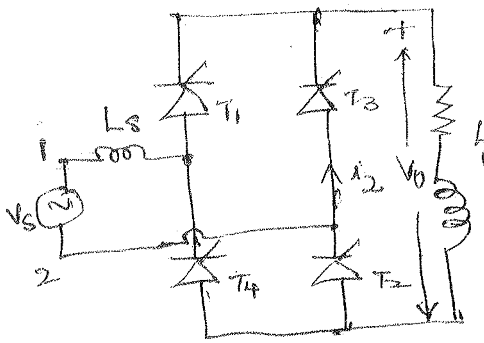
During commutation period, the output or load voltage will be average of conducting phase 1ϕ $V_o = 0$, 3ϕ $V_o = \frac{V_a + V_b}{2}$

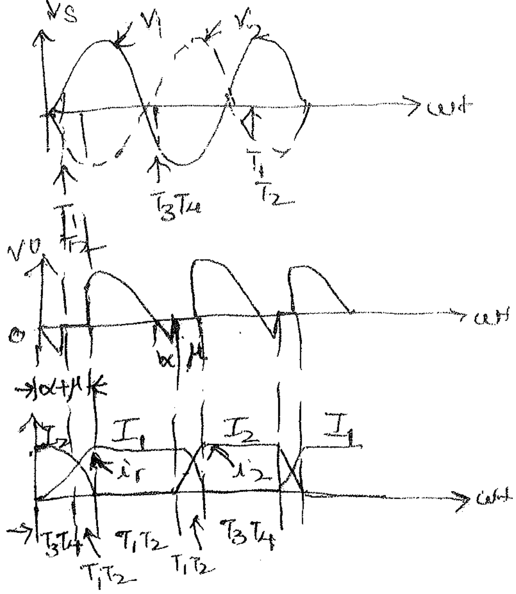
μ - overlapping angle.

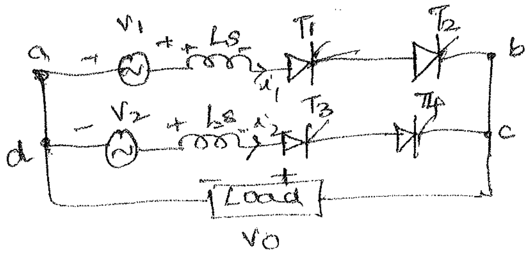
The commutation period in seconds when outgoing and incoming SCRs are conducting is known as the overlap period. The angular period during which the incoming and outgoing SCRs are conducting & known as commutation angle or overlap angle μ in degrees or radians.

Single phase full converter

The commutation overlap will be more in full converters than semiconverters. In 1ϕ full source, L_s is the source inductance. The load current is assumed constant. When terminal 1 of source voltage V_s is ... I load and T_1 ; IIIly when terminal 2







Apply KVL for abcda

$$V_1 - L_s \frac{di_1}{dt} + L_s \frac{di_2}{dt} - V_2 = 0$$

$$V_1 - V_2 = L_s \left[\frac{di_1}{dt} - \frac{di_2}{dt}\right]$$

$V_1 = V_m \sin\omega t \quad V_2 = -V_m \sin\omega t$

Apply laplace

$$\left[V_m \sin\omega t + V_m \sin\omega t\right] = L_s\left[s I(s) - s I_2(s)\right]$$

$$L_s\left[\frac{di_1}{dt} - \frac{di_2}{dt}\right] = 2V_m \sin\omega t$$

$$i_1 + i_2 = 0$$

As the load current is Constant

$$\frac{di_1}{dt} + \frac{di_2}{dt} = 0$$

$$\frac{di_1}{dt} = -\frac{di_2}{dt}$$

$$L_s 2\left[\frac{di_1}{dt}\right] = 2 V_m \sin\omega t$$

$$\frac{di_1}{dt} = \frac{V_m}{L_s} \sin\omega t$$

The current i_1 through T_1, T_2 builds up from 0 to I_0 during the overlapping angle μ.

(ie) at $\omega t = \alpha$, $i = 0$ at $\omega t = \alpha + \mu$, $i = I_0$

$$\int_0^{I_0} di_1 = \frac{V_m}{L_s} \int_{\alpha/\omega}^{(\alpha+\mu/\omega)} \sin\omega t \, d\omega t$$

$$= \frac{V_m}{L_s}\left[-\cos\omega t\right]_{\alpha/\omega}^{\alpha+\mu/\omega}$$

$$= \frac{V_m}{\ } \left[-\cos(\alpha+\mu) + \cos\alpha\right]$$

$$V_o = \frac{V_m}{\pi}\int_{\alpha+\mu}^{\alpha+\pi} \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi}\left(-\cos\omega t\right]_{\alpha+\mu}^{\alpha+\pi} = \frac{V_m}{\pi}\left[-\cos(\alpha+\pi)+\cos(\alpha+\mu)\right]$$

$$V_o = \frac{V_m}{\pi}\left[\cos(\alpha+\mu) + \cos\alpha\right] \quad \text{—— (2)}$$

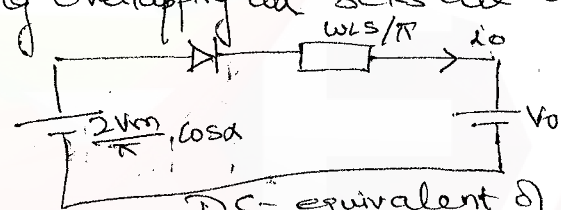
from (1) & (2)

$$\cos(\alpha+\mu) = \cos\alpha - \left(\frac{\omega L_s I_o}{V_m}\right)$$

$$V_o = \frac{V_m}{\pi}\left[\cos\alpha + \cos\alpha - \left(\frac{\omega L_s I_o}{V_m}\right)\right]$$

$$V_o = \frac{2V_m}{\pi}\cos\alpha - \frac{\omega L_s I_o}{\pi}$$

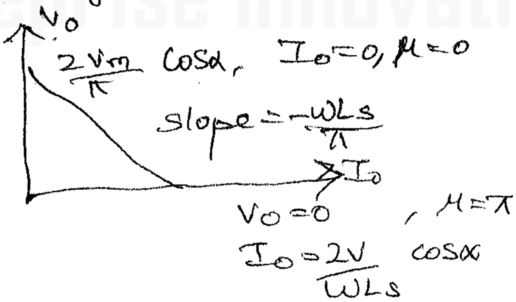
During overlapping all SCRs are Conducting



DC equivalent of 1φ full converter

Diode merely indicates, load current is unidirectional. Effect of source inductance L_s is to present an equivalent resistance of magnitude $\omega L_s/\pi$ in series with internal voltage of rectifier $2V_m/\pi \cos\alpha$.

Voltage drop due to L_s is proportional to I_o and L. As I_o increases, commutation interval or overlap angle increases, so the average o/p voltage decreases.



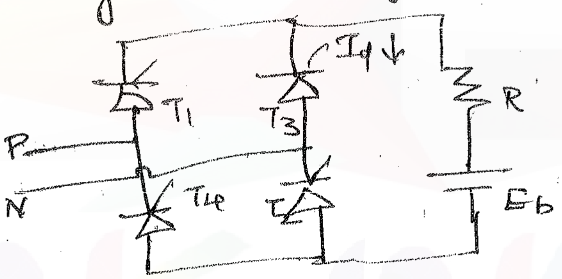
when $\mu = \pi$, load will be short circuited permanently, so $V_o = 0$, since all SCR are conducting.

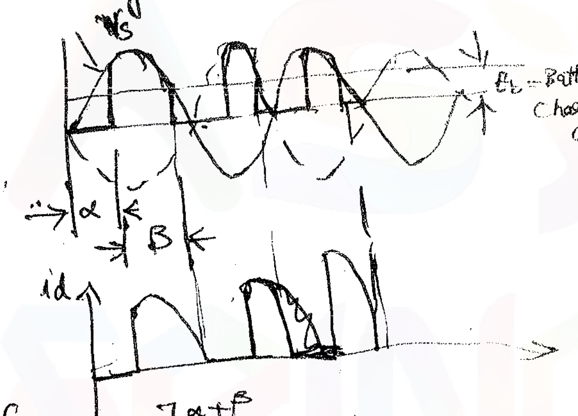
Performance of Converter Circuits with Battery load or Effect of Load Inductance

For converters to be used as regulated dc power supplies, an output filter is required to reduce the ripple in direct current and voltage of the load. So Inductance L is made reasonably large to act as filter choke. But there are applications in which o/p voltage is not filtered and only the rectified voltage is used. So the load current will not be constant.

The voltage and current waveforms for single phase fully controlled bridge has been discussed previously with purely resistive load, L is Zero. Load current is discontinuous since SCR turns off by Natural Commutation.

Load current is not only decided by the firing angle, but also by the battery load E.





Average o/p voltage

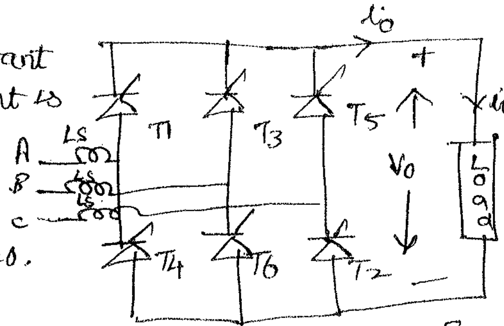
$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\alpha+\beta} V_m \sin\omega t \, d\omega t = \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\alpha+\beta}$$

$$= \frac{V_m}{\pi}\left[\cos\alpha - \cos(\alpha+\beta)\right]$$, β is Conduction angle.

$$\alpha+\beta = \pi - \sin^{-1}\left[\frac{E_b}{V_m}\right]$$

Effect of source inductance on. Three phase full Converter bridge

The load current is assumed constant as the analysis with pulsating current is quite complicated.

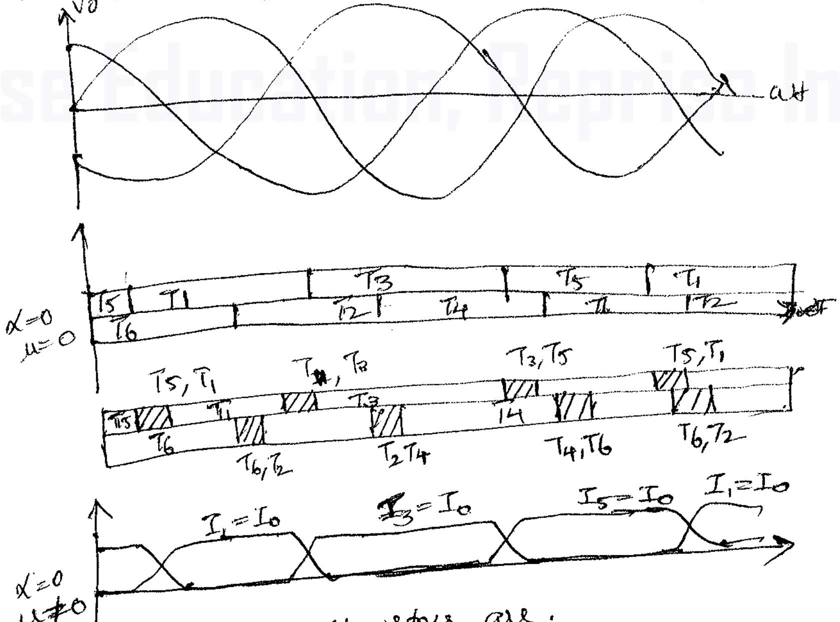


The conduction of various SCRs with firing angle $\alpha = 0$ and overlap angle $\mu = 0$.

$T_5 T_6$ conduct upto $30°$,
$T_1 T_6$ from $30°$ to $90°$.
$T_1 T_2$ from $90°$ to $150°$

Two SCRs Conduct at a time, One from positive group and other from negative group.

For the effect of overlap, from $\omega t = 0$ to $30°$, $T_5 T_6$ conduct. At $\omega t = 30°$, T_5 is outgoing SCR, T_1 is incoming SCR and both T_5, T_1 belong to positive group. As T_1 is triggered Current through T_5 starts decaying while through T_1 current begins to build up. At $\omega t = 30° + \mu$, I_5 is zero, while $I_1 = I_0$. After $\omega t = 30$ to $\omega t = 30°$ to $30 + \mu$, three SCRs, T_5, T_6, T_1 conduct. After $\omega t = 30$ to $30 + \mu$, T_6, T_1 Conduct. At $\omega t = 90°$, T_2 is triggered I_6 begins to decrease and I_2 starts to build up. Therefore from $\omega t = 90°$ to $90 + \mu$, three SCRs T_6, T_1, T_2 conduct. At $\omega t = 90 + \mu$, $I_6 = 0$, $I_2 = I_0$. After $\omega t = 90 + \mu$, only two SCRs T_1, T_2 conducts. When positive group of SCRs are undergoing Commutation, two SCRs from positive group and one SCR from negative group. Illy for negative group of SCR.



... various thyristors are.

This means that voltage from $\omega t = 30°$ to $30 + \mu$ follow the curve $\frac{V_a + V_c}{2}$ from the positive group. During commutation of T_6, T_2 the voltage waveform the negative group $\frac{V_b + V_c}{2}$.

The effect of source inductance L_s is reduce the average dc o/p voltage. The average value of fall in o/p voltage due to overlap

$$= \frac{3}{\pi}\int_0^{\mu} V_L \, d(\omega t) = \frac{3}{\pi}\int_0^{\mu} L_s \frac{di}{dt} \, d(\omega t)$$

$$= \frac{3L_s}{\pi}\int_0^{\mu/\omega} \frac{\omega di}{dt} dt = \frac{3\omega L_s}{\pi}\int_0^{I_o} di = \frac{3\omega L_s}{\pi} I_o .$$

O/p voltage with no overlap = internal voltage of the 3-phase full converter

$$= \frac{3V_{ml}}{\pi}\cos\alpha$$

o/p voltage with overlap $V_0 = \frac{3V_{ml}}{\pi}\cos\alpha - \frac{3\omega L_s}{\pi} I_o$

for m-pulse converter, fall in o/p voltage due to overlap

$$= \frac{m}{2\pi}\int_0^{\mu} L_s\left(\frac{di}{dt}\right) d(\omega t) = \frac{m\omega L_s}{2\pi}\int_0^{\mu/\omega}\left(\frac{di}{dt}\right) dt$$

$$= \frac{m\omega L_s}{2\pi}\int_0^{I_o} di = \frac{m\omega L_s I_o}{2\pi}$$

for 2-pulse converter, voltage drop due to overlap $= \frac{\omega L_s}{\pi} I_o$

for 6-pulse converter, voltage drop due to overlap $= \frac{3\omega L_s}{\pi} I_o$

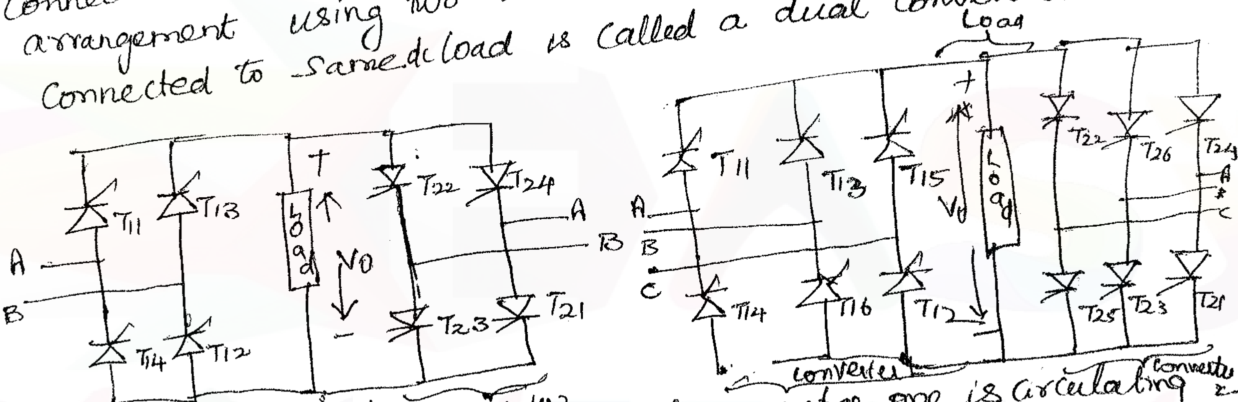
o/p voltage for a 3-phase full converter,

$$V_0 = \frac{3V_{ml}}{\pi}\cos(\alpha+\mu) + \frac{3\omega L_s}{\pi} I_o .$$

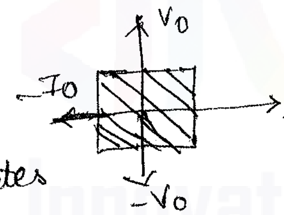
Dual Converters:

Semi Converters are Single quadrant converters. This means the entire firing angle range, load voltage and current have one polarity. In full converters, direction of current cannot be reversed because of unidirectional properties of SCRs but polarity of o/p voltage can be reversed. Full converter operates as a rectifier in first quadrant, from $\alpha = 0$ to 90° and as an inverter, from $\alpha = 90^\circ$ to 180° in fourth quadrant.

In case four quadrant operation is required without any mechanical change over switch, two full converters can be connected back to back to the load circuit. Such an arrangement using two full converters in antiparallel and connected to same dc load is called a dual converters.



Two functional modes of a dual converter, one is circulating current mode and the other is non circulating current mode.



The converter 1 works in first and fourth quadrant. The converter 2 works in second and third quadrant. So a dual converter operates in four quadrant operation.

Ideal Dual Converter:

When the Dual converter is ideal, there is no ripple in their output voltage. V_{01} and V_{02} are the magnitudes of average o/p voltage of converters 1 and 2 respectively. V_{01} and V_{02} show with the dc voltage sources. D_1 and D_2 indicates the unidirectional flow of current. The firing angles of both the converters are controlled in such a manner that the average output voltage of converters are equal in magnitude and have same polarity.

$$V_{01} = V_{max} \cos\alpha_1 \quad , V_{02} = V_{max} \cos\alpha_2$$

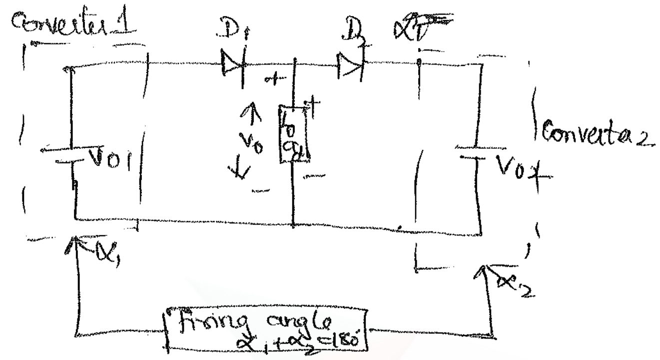
Under normal operation, V_{01} has upper positive and lower negative polarities and V_{02} has upper negative and lower positive polarities.

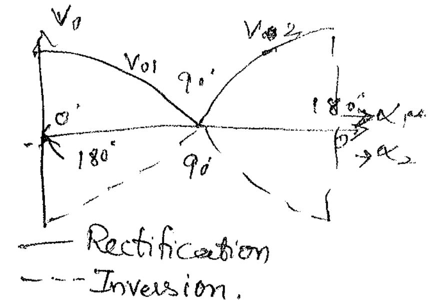
$$V_0 = V_{01} = -V_{02}.$$

$$V_{max}\cos\alpha_1 = -V_{max}\cos\alpha_2$$

$$\cos\alpha_1 = -\cos\alpha_2 = \cos(180-\alpha_2)$$

$$\alpha_1 + \alpha_2 = 180°$$





Practical Dual Converter:

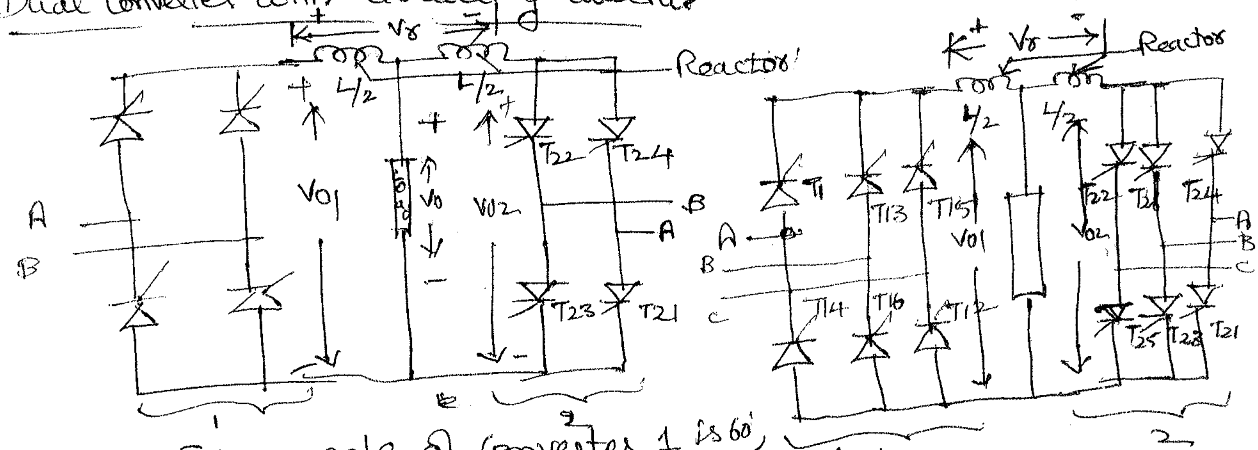
The firing angle $\alpha_1+\alpha_2=180°$ and with both the converter in operation, their average output voltages are equal and have the same polarity. One converter will be operating as rectifier with firing angle α_1 and other as inverter with firing angle $(180-\alpha_1)$. So the average o/p voltage will be out of phase. So a large circulating current flows between the two converters but not through load.

Dual Converter without Circulating current:

Only one converter is in operation at a time and it alone carries the entire load current. Only this converter receives the firing pulse from trigger control.

Suppose converter 1 is in operation, and now converter 2 has to be made on. Then the firing pulse to converter 1 has to be removed or firing angle of converter 1 to maximum value and then its firing pulse are blocked. With this load current decay to zero so the converter 2 is made to conducting, but now the current through the converter build up through load in reverse direction. The load current must be decayed to zero when the converter is changing from 1 to 2 or 2 to 1. A time delay of 10 to 20 msec is introduced before the firing pulse are applied to incomming converter.

Dual Converter with Circulating Current:



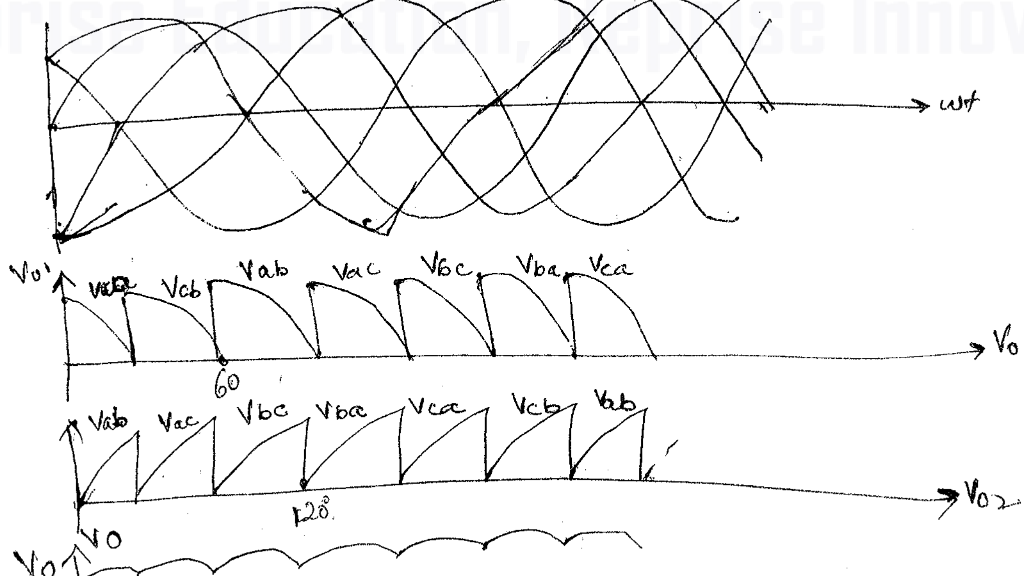
If the firing angle of converter 1 is 60°, then the firing angle of converter 2 must be 120°. So the firing angle of converter 1 is acting as rectifier and converter 2 as inverter. The o/p voltage of converter 1 and 2 has the same average value but the instantaneous o/p voltage will be not similar as Vo1 and Vo2. So circulating current flows between the converters. This circulating current is limited by a reactor. If the load current is reversed, the role of two converters is interchanged. This can be done by making converter 1 acting as inverter and converter 2 as rectifier. so $\alpha_1 + \alpha_2 = 180°$.

The main disadvantage ... of dual converter are

(i) A reactor is required to limit the circulating current. The size and cost of this reactor may be quite significant at high power levels.

(ii) Circulating current gives rise to more losses in the converters, hence the efficiency and power factor are ... low.

iii) Converters have to handle load as well as circulating currents.



The reactor is assumed lossless

Firing angle of two converters are $\alpha_1 + \alpha_2 = 180^\circ$

if α_1 be equal to 60°, $\alpha_2 = 180 - 60^\circ = 120^\circ$,

The load voltage V_0 is equal to the average value of the instantaneous converter output voltage V_{01} and V_{02}.

$$V_0 = V_{01} + V_{02}$$

$\omega t = 0^\circ$ $\quad V_0 = \frac{V_{ml} \sin 60^\circ + 0}{2} = 0.433 V_{ml}$

$\omega t = 30^\circ$ $\quad V_0 = \frac{V_{ml} \sin 30 + V_{ml} \sin 30}{2} = 0.5 V_{ml}$. ~~$V_{ml}$~~

$\omega = 60^\circ$ $\quad V_0 = \frac{0 + V_{ml} \sin 60}{2} = 0.433 V_{ml}$

The reactor voltage V_r is equal to the difference of converter o/p vo

$$V_r = V_{01} - V_{02}$$

$\omega t = 0$ $\quad V_r = V_{ml} \sin 60^\circ - 0 = 0.866\, V_{ml}$

$\omega t = 30^\circ$ $\quad V_r = V_{ml} \sin 30 - V_{ml} \sin 30 = 0$

$\omega t = 60^\circ$ $\quad V_r = 0 - V_{ml} \sin 60^\circ = -0.866\, V_{ml}$.

$V_r = L \frac{di_c}{dt}$ $\quad i_c$ is the circulating current through both the converters and reactor L.

$\omega t = 0^\circ$, V_r is maximum positive slope of i_c is maximum and po

On-Load: The converter 1 current is $i_1 = I_0 + i_c$.

$$V_{01} = V_{ab} \quad V_{02} = V_{bc}$$

$$V_r = V_{01} - V_{02} = V_{ab} - V_{bc}$$

$V_{ab} = V_{ml} \sin \omega t$ $\quad$ As V_{bc} lags V_{ab} by 120°.

$$V_{bc} = V_{ml} \sin(\omega t - 120^\circ)$$

$$V_r = V_{ml} [\sin \omega t - \sin(\omega t - 120^\circ)]$$

$$V_r = \sqrt{3} V_{ml} \sin(\omega t + \pi/6).$$

$$i_c = \frac{1}{L} \int_{(\alpha_1 + \pi/3)/\omega}^{t} V_r \, dt = \frac{\sqrt{3} V_{ml}}{L} \int_{(\alpha_1 + \pi/3)/\omega}^{t} \sin(\omega t + \pi/6) dt.$$

$$i_c = \frac{\sqrt{3} V_{ml}}{\omega L} \int_{\alpha_1 + \pi/3}^{\omega t} \sin(\omega t + \pi/6)\, d\omega t \qquad i_c = \frac{\sqrt{3} V_{ml}}{\omega L} \left[-\sin \alpha_1 - \cos(\omega t + \pi/6) \right]$$

The peak value of circulating current occurs when $\omega t = 5\pi/6$

$$i_{cp} = \frac{\sqrt{3} V_{ml}}{\omega L} [1 - \sin \alpha_1]$$

The peak value of firing angle depends upon firing angle α_1.

for $\alpha_1 = 0$, $i_{cp} = \sqrt{3} V_{ml} / \omega L$ $\quad$ for $\alpha_1 = 90^\circ$, $i_{cp} = 0$.

Gate Circuit schemes for Phase Control.

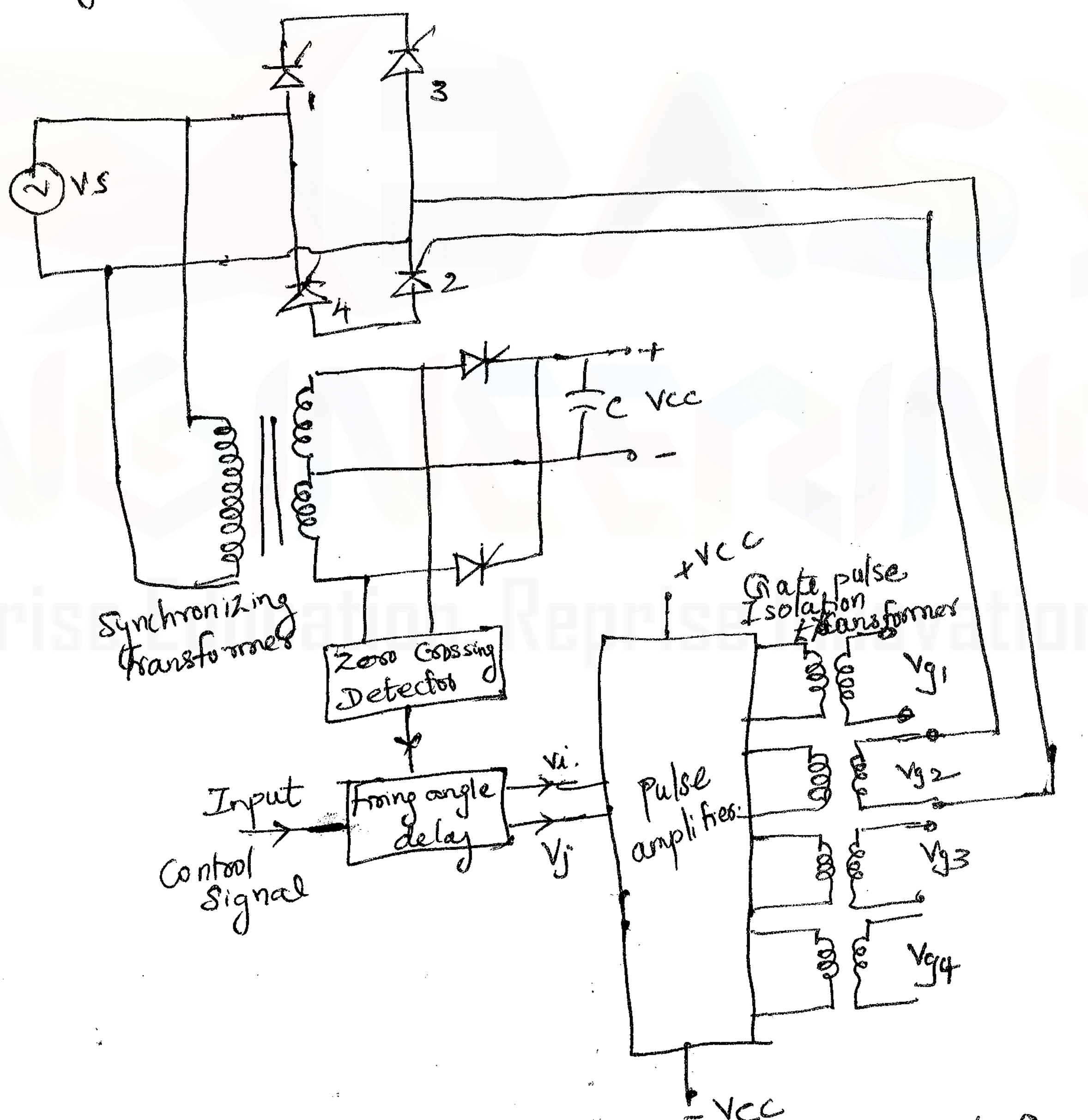
A gate trigger Circuit for thyristors in phase Controlled rectifiers should possess the following

(i) A circuit for the detection of zero crossing of the input voltage

(ii) Generation of triggering pulse of required wave shape.

(iii) DC power supply for pulse amplifiers

(iv) Gate trigger circuit isolation from line potential by means of pulse transformers or opto couplers.



* The gating circuit consists of synchronizing transformer, diode rectifier, zero crossing detector, firing angle delay, pulse amplifier, gate isolation transformer, and power circuit for converter.

* Synchronizing step down transformer steps down supply voltage suitable for zero crossing detector (z... and for delivering dc supply to gate trigger circuit.

* ZCD converts ac synchronizing i/p voltage into ramp voltage and synchronize with zero crossing ac supply voltage.

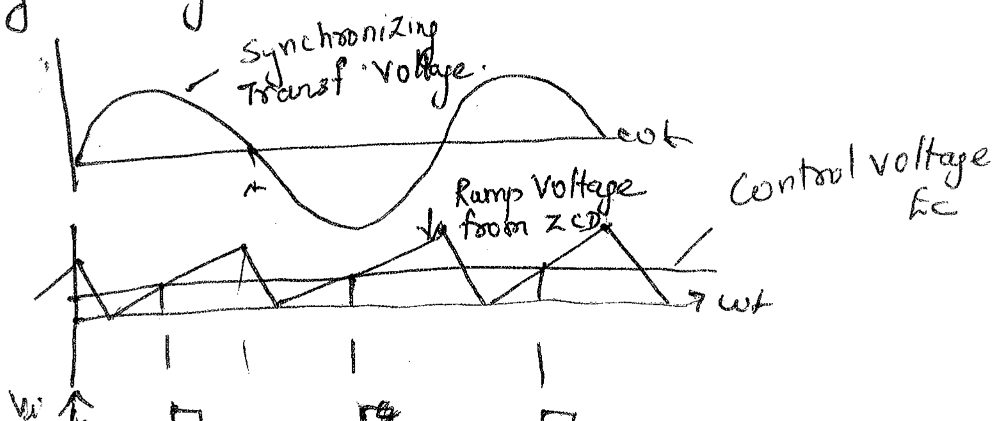
* In firing angle delay block, the constant amplitude ramp voltage is compared with control signal Vc...

* When rising ramp voltage equals control voltage ... a pulse signal of controlled duration is generated. These signals are indicated as V_i for thyristors 1 and 2, V_j for thyristors 3 and 4.

* If Ec is lowered, firing angle decrease and if Ec increases, firing angle increases.

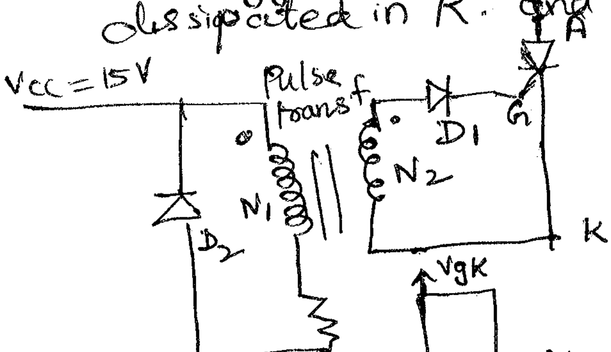
* Firing angle delay is proportional to control signal voltage Ec.

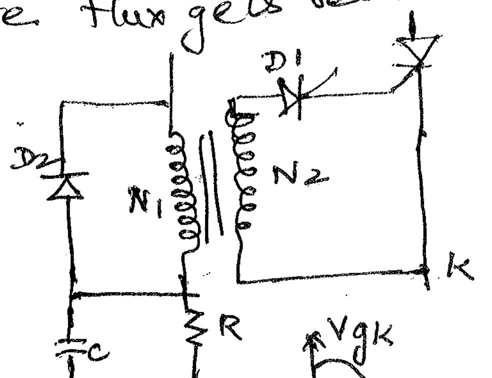
* The pulse o/p from firing angle delay is fed to the pulse amplifier where it is amplified and then used for triggering the thyristors using isolation transformers.



Gate Pulse amplifiers:-

* Consists of MOSFET, a pulse transformer for isolation and diodes D_1, D_2'.
* when a Voltage of appropriate level is applied to the gate of MOSFET, it gets turned on.
* Most of the dc voltage V_{cc} appears across transformer primary and corresponding pulse voltage is induced in the transformer secondary.
* Amplified pulse on secondary side is appled to gate of thyristor to turn it on.
* When MOSFET gate signal goes zero, MOSFET is turned off.
* Primary current and flux in core tends to decrease. Due to this a voltage of opposite polarity is induced in both primary and secondary windings of pulse transformer.
* Diode D_1 prevents the flow of negative current due to reverse secondary voltage when MOSFET turns off.
* Reverse voltage in primary however forward biased diodes D_2 when MOSFET turns off.
* Current flow is established in the circuit consisting of primary ~~Energy in transformer~~, R and D_2.
* Energy in transformer magnetic core gets dissipated in R and core flux gets reset.

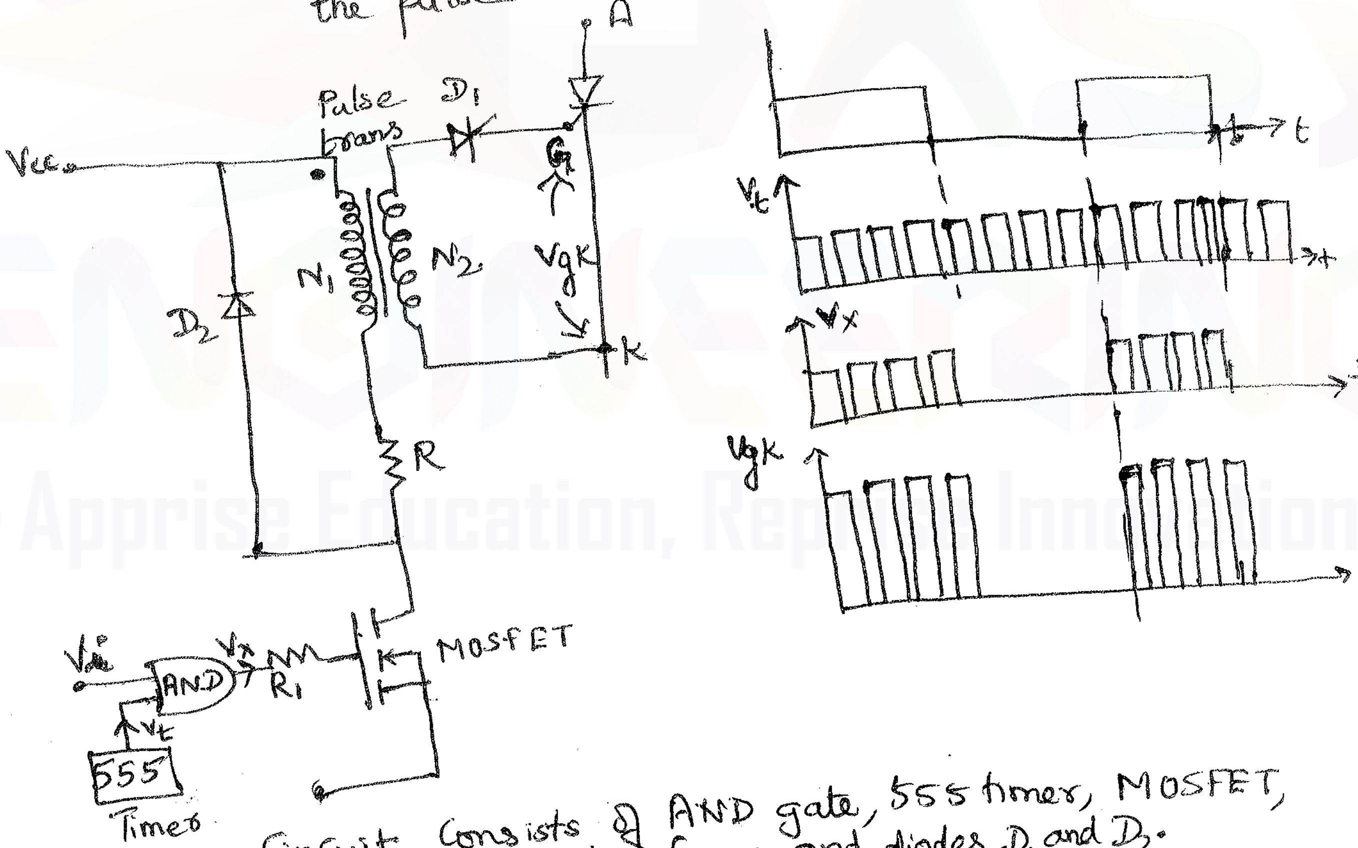




* If pulse width at the secondary terminals is to be increased, then a Capacitor C is Connected across R.

Pulse train gating:-

* Continuous gating suffers from some disadvantages like increased thyristor losses and distortion of output pulse due to saturation of pulse transformer by continuous pulse.
* To overcome these problems a train of firing pulses is used to turn on a thyristor.
* Pulse train gating signal is also called High frequency carrier gating.
* Pulse train can be generated by modulating the pulse width at a high frequency.



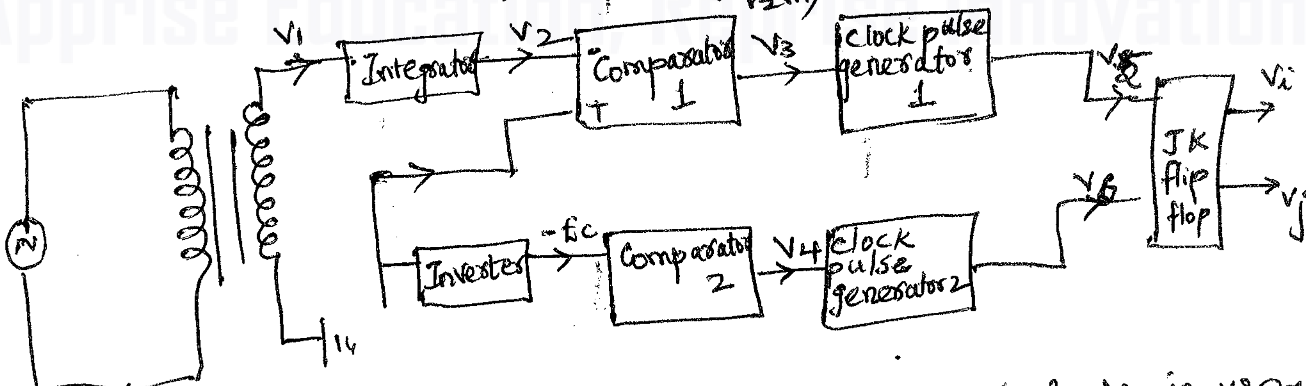
* Circuit Consists of AND gate, 555 timer, MOSFET, isolation pulse transformer and diodes D_1 and D_2.
* Pulse signal from thyristor trigger and output of 555 timer is fed to AND gate to get waveform o/p V_x
* Duty cycle of timer should be less than 50% ... the transformer flux to reset.

Cosine firing scheme:

* The synchronizing transformer steps down the supply voltage to an appropriate level.
* The o/p voltage V_1 of synchronizing transformer is integrated to get cosine wave V_2.
* The dc control voltage E_c varies from maximum positive E_{cm} to maximum negative E_{cm} so that firing angle can be varied from zero to 180°
* Cosine wave V_2 is compared with comparator 1 and 2 with E_c and $-E_c$.
* When E_c is high compared to V_2, o/p voltage V_3 is available from comparator 1.
* IIIly for comparator 2
* Comparator 1 and 2 gives the output pulse V_3 and V_4 respectively.
* firing angle is governed by intersection of V_2 and E_c.
* When E_c is maximum, firing angle is zero.
  When E_c is maximum value of cosine signal V_2.
  V_{2m} – maximum

$$V_{2m} \cos\alpha = E_c$$

$$\alpha = \cos^{-1}\left(\frac{E_c}{V_{2m}}\right)$$



* for single phase full converter, the signal V_i is used to turn on the SCRs in positive half cycle.
  ... to trigger SCR in negative

$$V_0 = \frac{2V_m}{\pi} \cos\left[\cos^{-1} \frac{E_c}{V_{2m}}\right]$$

$$= \left[\frac{2V_m}{\pi} \cdot \frac{1}{V_{2m}}\right] E_c$$

$$V_0 = K E_c$$

* Cosine firing scheme provides a linear transfer characteristics between the o/p voltage V_0 and control voltage E_c.