MOHAMED SATHAK A J COLLEGE OF ENGINEERING

Siruseri IT Park, OMR, Chennai - 603103

LESSON PLAN

Department of Electrical and Electronics Engineering

Name of the Subject	DIGITAL LOGIC CIRCUITS	Name of the handling Faculty	Mr. S.V.Vinodh
Subject Code	EE3302	Year / Sem	II/III
Acad Year	2022-23	Batch	2021-25

Course Objective

To introduce the fundamentals of combinational and sequential digital circuits.

To study various number systems and to simplify the mathematical expressions using Boolean functions word problems

To study implementation of combinational circuits using Gates` and MSI Devices.

To study the design of various synchronous and asynchronous circuits

To introduce digital simulation techniques for development of application oriented logic circuit

Course Outcome

At the end of the course, the students will be able to

CO1: Explain various number systems and characteristics of digital logic families

CO2: Apply K-maps and Quine McCluskey methods to simplify the given Boolean expressions

CO3: Explain the implementation of combinational circuit such as multiplexers and de multiplexers - code converters, adders, subtractors, Encoders and Decoders

CO4: Design various synchronous and asynchronous circuits using Flip Flops

CO5: Explain asynchronous sequential circuits and programmable logic devices

CO6: Use VHDL for simulating and testing RTL, combinatorial and sequential circuits

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB / PPT / NPTEL / MOOC / etc)	Blooms Level (L1-L6)	CO	PO
UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES							
1	**Review of number systems**	**T1, R2**	**1**	**BB**	**L1**	C01	PO1-PO3,PO12
2	**Binary codes, Error detection codes**	**T1, R2**	**1**	**BB**	**L3**	C01	PO1-PO3,PO12
3	**Error correction codes (Parity and Hamming code)**	**T1, R2**	**1**	**BB**	**L3**	C01	PO1-PO3,PO12
4	**Minimization using K maps**	**T1, R2**	**1**	**BB**	**L2**	CO2	PO1-PO3
5	**Qunine McCluskey method**	**T1, R2**	**1**	**PPT**	**L2**	CO2	PO1-PO3
6	**Digital Logic Families: RTL,DTL-operation**	**T1, R2**	**1**	**PPT**	**L2**	CO2	PO1-PO3
7	**ECL,MOS families -operation**	**T1, R2**	**1**	**PPT**	**L2**	CO2	PO1-PO3
8	**TTL Operation**	**T1, R2**	**1**	**BB**	**L2**	CO2	PO1-PO3
9	**Comparison of RTL, DTL, TTL, ECL and MOS families, characteristics of digital logic family**	**T1, R2**	**1**	**BB**	**L2**	CO2	PO1-PO3

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any

1. Tutorial - 1 on nubering systems
2. Tutorial - 2 on error detection
3. Tutorial - 3 on digital logic families

Evaluation method

Based on tutorial marks

UNIT II COMBINATIONAL CIRCUITS							
10	**Combinational logic circuits**	**T2, R1**	**1**	**BB/NPTEL**	**L2**	CO2	PO1-PO3,PO12
11	**Representation of logic functions**	**T2, R1**	**1**	**BB**	**L2**	CO2	PO1-PO3,PO12
12	**SOP and POS forms**	**T2, R1**	**1**	**BB**	**L3**	CO2	PO1-PO3,PO12
13	**K-map representations**	**T2, R1**	**1**	**BB/NPTEL**	**L3**	CO2	PO1-PO3,PO12
14	**Minimization using K maps**	**T2, R1**	**1**	**BB/NPTEL**	**L3**	CO2	PO1-PO3,PO12
15	**Simplification and implementation of combinational logic**	**T2, R1**	**1**	**PPT**	**L3**	CO2	PO1-PO3,PO12
16	**Multiplexers and demultiplexers**	**T2, R1**	**1**	**PPT**	**L3**	CO2	PO1-PO3,PO12
17	**Code converters**	**T2, R1**	**1**	**PPT**	**L3**	CO2	PO1-PO3,PO12
18	**Adders, subtractors, Encoders, Decoders**	**T2, R1**	**1**	**BB**	**L3**	CO2	PO1-PO3,PO12

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any

1. Tutorial - 1 on Combinational logic circuits
2. Tutorial - 2 on K-map representations
3. Tutorial - 3 on Minimization using K maps
4. Assignment on K-map problems

Evaluation method

1. 10 marks for assignment

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS							
18	**Sequential logic- SR, JK flip flops**	**T1, R3**	**1**	**BB/NPTEL**	**L2**	CO3	PO1-PO3
19	**D and T flip flops –working Principles,Truth table,Excitation Table**	**T1, R3**	**1**	**BB**	**L2**	CO3	PO1-PO3
20	**Level triggering and edge triggering of flip flops**	**T1, R3**	**1**	**BB**	**L2**	CO3	PO1-PO3
21	**Counters - asynchronous type**	**T1, R3**	**1**	**BB**	**L3**	CO3	PO1-PO3
22	**Counters - synchronous type**	**T1, R3**	**1**	**BB**	**L3**	CO3	PO1-PO3
23	**Modulo counters**	**T1, R3**	**1**	**PPT**	**L3**	CO3	PO1-PO3
24	**Shift registers**	**T1, R3**	**1**	**PPT**	**L3**	CO3	PO1-PO3
25	**Design of synchronous sequential circuits – Moore and Melay models**	**T1, R3**	**1**	**PPT**	**L4**	CO3	PO1-PO3
26	**Counters, state diagram; state reduction; state assignment.**	**T1, R3**	**1**	**PPT**	**L3**	CO3	PO1-PO3

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any

MCQ Quiz on Synchronous Sequential Circuits

Evaluation method

MCQ marks

UNIT IV Asynchronous Sequential Circuits and Programmable Logic Devices							
27	**Asynchronous sequential logic circuits**	**T1, R5**	**1**	**BB**	**L2**	C03	PO1-PO3
28	**Transition table, flow table**	**T1, R5**	**1**	**BB**	**L2**	C03	PO1-PO3
29	**Race conditions**	**T1, R5**	**1**	**BB**	**L2**	C03	PO1-PO3
30	**Hazards in digital circuits**	**T1, R5**	**1**	**BB**	**L1**	C03	PO1-PO3
31	**Errors in digital circuits**	**T1, R5**	**1**	**BB**	**L1**	C03	PO1-PO3
32	**Analysis of asynchronous sequential logic circuits**	**T1, R5**	**1**	**PPT**	**L3**	C03	PO1-PO3

33	**Introduction to Programmable Logic Devices:PROM**	**T1, R5**	**1**	**PPT**	**L2**	C04	PO1-PO5
34	**PLA,PAL**	**T1, R5**	**1**	**PPT**	**L2**	C04	PO1-PO5
35	**CPLD,FPGA**	**T1, R5**	**1**	**PPT**	**L2**	C04	PO1-PO5

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
MCQ Quiz on Asynchronous Sequential Circuits and Programmable Logic Devices

Evaluation method
Quiz marks

UNIT V VHDL

36	**RTL Design**	**T2, R2, R4**	**1**	**BB**	**L3**	CO2	PO1-PO3
37	**Combinational logic circuit**	**T2, R2, R4**	**1**	**BB**	**L3**	CO2	PO1-PO3
38	**Sequential circuit**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO3	PO1-PO3
39	**Operators**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO3
40	**Introduction to Packages**	**T2, R2, R4**	**1**	**PPT**	**L1**	CO5	PO1-PO3
41	**Subprograms**	**T2, R2, R4**	**1**	**PPT**	**L2**	CO5	PO1-PO3
42	**Test bench, Revision**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO3
43	**Simulation /Tutorial Examples: adders**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO5
44	**Simulation /Tutorial Examples: counters**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO5
45	**Simulation /Tutorial Examples: flip-flops**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO5
46	**Simulation /Tutorial Examples: FSM**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO5
47	**Simulation /Tutorial Examples:Multiplexers/Demultiplexers**	**T2, R2, R4**	**1**	**PPT**	**L3**	CO5	PO1-PO5

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any
Assignment on VHDL program

Evaluation method
Marks for assignment

Content Beyond the Syllabus Planned

1	**The process of Analog to Digital conversion and Digital to Analog conversion**
2	**Digital Integrated Circuit Tester Using (AT89S52) micro controller**

Text Books

1	**James W. Bignel, Digital Electronics, Cengage learning, 5th Edition, 2007.**
2	**M. Morris Mano, 'Digital Design with an introduction to the VHDL', Pearson Education, 2013**
3	**Comer "Digital Logic & State Machine Design, Oxford, 2012**

Reference Books

1	**Mandal, "Digital Electronics Principles & Application, McGraw Hill Edu, 2013.**
2	**William Keitz, Digital Electronics-A Practical Approach with VHDL, Pearson, 2013.**
3	**Thomas L.Floyd, 'Digital Fundamentals', 11th edition, Pearson Education, 2015.**
4	**Charles H.Roth, Jr, Lizy Lizy Kurian John, 'Digital System Design using VHDL, Cengage, 2013.**
5	**D.P.Kothari,J.S.Dhillon, 'Digital circuits and Design',Pearson Education, 2016.**

Website / URL References

1	https://www.youtube.com/watch?v=sUutDs7FFeA NPTEL Lecture 3 Combinational Logic Basics
2	https://www.youtube.com/watch?v=EznCqZ1eh5Q&feature=emb_title Lecture 6 - Karnaugh Maps And Implicants
3	https://www.youtube.com/watch?v=2ecMG_OciLo&feature=emb_title Lecture 17 - S-R,J-K and D Flip Flops

Blooms Level										
Level 1 (L1) : Remembering Level 2 (L2) : Understanding Level 3 (L3) : Applying	Lower Order Thinking	Fixed Hour Exams	Level 4 (L4) : Analysing Level 5 (L5) : Evaluating Level 6 (L6) : Creating						Higher Order Thinking	Projects / Mini Projects
Mapping syllabus with Bloom's Taxonomy LOT and HOT										
Unit No	**Unit Name**	**L1**	**L2**	**L3**	**L4**	**L5**	**L6**	LOT	HOT	**Total**
Unit 1	**NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES**	1	6	2	0	0	0	9	0	9
Unit 2	**COMBINATIONAL CIRCUITS**	0	2	**7**	**0**	**0**	**0**	9	0	9
Unit 3	**SYNCHRONOUS SEQUENTIAL CIRCUITS**	0	3	**5**	**1**	**0**	**0**	8	1	9
Unit 4	**Asynchronous Sequential Circuits and Programmable Logic Devices**	2	6	**1**	**0**	**0**	**0**	9	0	9
Unit 5	**VHDL**	1	1	**10**	**0**	**0**	**0**	12	0	12
Total		4	18	25	1	0	0	47	1	48
Total Percentage		8.33333	37.5	52.0833	2.08333	0	0	97.9167	2.08333	100

CO PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	**3**	**2**	**2**									2	2	1
CO2	**3**	**3**	**2**									2	2	1
CO3	**3**	**3**	**3**										1	1
CO4	**3**	**3**	**2**	**2**	**2**								1	1
CO5	**3**	**2**	**2**	**1**	**1**								1	1
Avg	**2**	**2**	**2**	**2**	**2**							2	2	1

Justification for CO-PO mapping

CO1	**High correlation for PO1 medium correlation with PO2, PO3, PO12 because we are using bacis engineering knowledge in problem analysis and design which are needed learn in life-long**
CO2	**High correlation for PO1, PO2 medium correlation with PO3, PO12 because we are using bacis engineering knowledge in problem analysis and design which are needed learn in life-long**
CO3	**High correlation for PO1, PO2, PO3 because we are using bacis engineering knowledge in problem analysis and sign which are needed learn in life-long**
CO4	**High correlation for PO1, PO2 medium correlation with PO3, PO4, PO5 because we are using bacis engineering knowledge in complex problem analysis and design using modern tools.**
CO5	**High correlation for PO1 medium correlation with, PO2, PO3 low correlation with PO4, PO5 because we are using bacis engineering knowledge in complex problem analysis and design using modern tools.**

3	**High level**	**2**	**Moderate level**	**1**	Low level

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