MOHAMMED SATHAK A J COLLEGE OF ENGINEERING

Siruseri IT park, OMR, Chennai - 603103

LESSON PLAN			
Department of CSE and IT			
Name of the Subject	DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION	**Name of the handling Faculty**	JAYANTHI.E & Mrs.S.ANUSUYA
Subject Code	CS3351	**Year / Sem**	II/III
Acad Year	2022-2023	**Batch**	2021-2025

Course Objective

To analyze and design combinational circuits
To analyze and design sequential circuits
To understand the basic structure and operation of a digital computer
To study the design of data path unit, control unit for processor and to familiarize with the hazards
To understand the concept of various memorieas and I/O interfacing

Course Outcome

CO1:Design various combinational digital circuits using logic gates
CO2:Design sequential circuits and analyze the design procedures
CO3:State the fundamentals of computer systems and analyze the execution of an instruction
CO4:Analyze different types of control design and identify hazards
CO5:Identify the characteristics of various memory systems and I/O communication

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB / PPT / NPTEL / MOOC / etc)	Blooms Level (L1-L6)	CO	PO
UNIT I - COMBINATIONAL LOGIC							
1	Combinational Circuits	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO5
2	K-map simplifications	T1	1	BB	L3	CO1	PO1,PO2,PO3,PO4,PO5
3	Analysis and Design procedures	T1	1	BB	L3	CO1	PO1,PO2,PO3,PO4,PO5
4	Binary Adder	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO5,PO11
5	Binary Subtractor	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO5,PO11
6	Decimal Adder	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO5
7	Magnitude Comparator	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO5,PO9
8	Encoder and Decoder	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO5,PO10,PO11,PO12
9	Multiplexers and Demultiplexers	T1	1	BB	L2	CO1	PO1,PO2,PO3,PO4,PO12
11	Lab session -Verification of Boolean theorems using logic gates.	T1	2	DEMO	L3	CO1	PO1,PO2,PO3
15	Lab session-Design and implementation of combinational circuits using gates for arbitrary functions.	T1	4	DEMO	L3	CO1	PO1,PO2,PO3
19	Lab session-Implementation of 4-bit binary adder/subtractor circuits.	T1	4	DEMO	L3	CO1	PO1,PO2,PO3
21	Lab Session-Implementation of code converters.	T1	2	DEMO	L3	CO1	PO1,PO2,PO3
25	Lab Session-Implementation of BCD adder, encoder and decoder circuits	T1	4	DEMO	L3	CO1	PO1,PO2,PO3
27	Lab Session-Implementation of functions using Multiplexers.	T1	2	DEMO	L3	CO1	PO1,PO2,PO3

Suggested Activity: Assignment / Case Studies / Tutorials/ Quiz / Mini Projects / Model Developed/others Planned if any DESIGN AND CRITICAL THINKING							
Evaluation method : MARKS WILL BE GIVEN BASED ON THEIR PRESENTATION							
UNIT II -SYNCHRONOUS SEQUENTIAL LOGIC							
28	Introduction to sequential circuits	T1	1	BB	L2	CO2	PO1,PO2,PO3,PO4,PO5
29	Flip flops- operation and excitation table	T1	1	BB	L2	CO2	PO1,PO2,PO3,PO4,PO5
30	Triggering of FF	T1	1	BB	L2	CO2	PO1,PO2,PO3
31	Analysis and design of clocked sequential circuits	T1,R1	1	BB	L2	CO2	PO1,PO2,PO3,PO4,PO5
32	Design- moore/ mealy models	T1	1	BB	L4	CO2	PO1,PO2,PO3,PO4,PO5
33	State minimization and State assignment	T1	1	BB	L3	CO2	PO1,PO2,PO3,PO4,PO5
34	Circuit implementation	T1,R1	1	BB	L3	CO2	PO1,PO2,PO3,PO4,PO5
35	Registers	T1	1	BB	L2	CO2	PO1,PO2,PO3,PO4,PO5
36	Counters	T1	1	BB	L2	CO2	PO1,PO2,PO3,PO4,PO5
42	Lab session-Implementation of the synchronous counters	T1	6	DEMO	L3	CO2	PO1,PO2,PO3
46	Lab sessiojn-Implementation of a Universal Shift register	T1	4	DEMO	L3	CO2	PO1,PO2,PO3
Suggested Activity: Assignment / Case Studies / Tutorials/ Quiz / Mini Projects / Model Developed/others Planned if any ASSIGNMENT-PROBLEMS BASED ON COUNTER DESIGN.							
Evaluation method : Marks will be awarded based on their performance.							

UNIT III- COMPUTER FUNDAMENTALS							
47	Functional units of a digital computer	T1	1	BB	L2	CO3	PO1,PO2
48	Von Neumann Architecture	T1,R1	1	BB	L2	CO3	PO1,PO2
49	operation and operands of computer hardware instructions	T1	1	BB	L2	CO3	PO1,PO2,PO4,PO5
50	Instruction set architecture(ISA)	T1	1	BB	L2	CO3	PO1,PO2,PO4,PO5,PO10
51	Memmory location, Address and operation	T1	1	BB	L2	CO3	PO1,PO2
52	Instruction and Instruction sequencing	T1,R1	1	BB	L2	CO3	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
53	Addressing modes	T1	1	BB	L2	CO3	PO1,PO2
54	Encoding of machine instruction	T1	1	BB	L2	CO3	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
55	Interaction between Assembly and high level language	T1	1	BB	L2	CO3	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
57	Lab session-Simulator based study of Computer Architecture	T2	2	PPT	L2	CO3	PO1,PO2
Suggested Activity: Assignment / Case Studies / Tutorials/ Quiz / Mini Projects / Model Developed/others Planned if any QUIZ							
Evaluation method : Marks will be given based on their responses							
UNIT IV- PROCESSOR							
58	Introduction	T1	1	BB	L2	CO4	PO1,PO2,PO3
59	Instruction Execution	T1	1	BB	L2	CO4	PO1,PO2,PO3,PO4,PO5
60	Building a data path	T1	1	BB	L2	CO4	PO1,PO2,PO3,PO4,PO5,PO6,PO7
61	Designing a control unit	R2,T1	2	BB	L2	CO4	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
62	Hardwired control	R2	1	BB	L2	CO4	PO1,PO2,PO3,PO4,PO5
63	Microprogrammed control	R2	1	BB	L2	CO4	PO1,PO2,PO3,PO4,PO5
64	Pipelining	R2	1	BB	L2	CO4	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
65	Data hazard	R2	1	BB	L2	CO4	PO1,PO2,PO3,PO4,PO5
66	Control Hazards	R2	1	BB	L2	CO4	PO1,PO2,PO3,PO4,PO5
Suggested Activity: Assignment / Case Studies / Tutorials/ Quiz / Mini Projects / Model Developed/others Planned if any MIND MAPPING							
Evaluation method : Marks will be awarded based on their responses.							
UNIT V-MEMORY AND I/O							
67	Memory concepts and Hierarchy	T1,R1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
68	Memory management	T1,R1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
69	Cache memories	T1,R1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
70	Mapping and replacement techniques	T1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
71	virtual memory	T1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
72	DMA -I/O	T1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
73	parallel and serial interface	R1	1	BB	L2	CO5	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
74	Interrupt I/O	R1	1	BB	L2	CO5	PO1,PO2,PO3,PO4,PO5
75	Interconnection standards:USB ,SATA	R1	1	BB	L2	CO5	PO1,PO2,PO4,PO5,PO9,PO10,PO 11,PO12
Suggested Activity: Assignment / Case Studies / Tutorials/ Quiz / Mini Projects / Model Developed/others Planned if any CASE STUDY							
Evaluation method : Marks will be given based on their presentation							

Content Beyond the Syllabus Planned	
1	Combinational circuits using Verilog HDL
2	ARM Processor

Text Books

1	M. Morris Mano, Michael D. Ciletti, "Digital Design : With an Introduction to the Verilog HDL, VHDL, and System Verilog", Sixth Edition, Pe
2	. David A. Patterson, John L. Hennessy, "Computer Organization and Design, The Hardware/Software Interface", Sixth Edition, Morgan Kaufm

Reference Books

1	Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, "Computer Organization and Embedded Systems", Sixth Edition, Tata McG
2	William Stallings, "Computer Organization and Architecture – Designing for Performance", Tenth Edition, Pearson Education, 2016.
3	M. Morris Mano, "Digital Logic and Computer Design", Pearson Education, 2016.

Website / URL References

1	https://nptel.ac.in/courses/117106086
2	https://ieeexplore.ieee.org/document/1463186
3	https://www.youtube.com/watch?v=AtfXJ0PNesk

Blooms Level

Level 1 (L1) : Remembering **Level 2 (L2) : Understanding** **Level 3 (L3) : Applying**	Lower Order Thinking	Fixed Hour Exams	**Level 4 (L4) : Analysing** **Level 5 (L5) : Evaluating** **Level 6 (L6) : Creating**	Lower Order Thinking	Higher Order Thinking	Projects / Mini Projects

Mapping syllabus with Bloom's Taxonomy LOT and HOT

Unit No	Unit Name	L1	L2	L3	L4	L5	L6	LOT	HOT	Total
Unit 1	COMBINATIONAL LOGIC	0	7	20	0	0	0	27	0	27
Unit 2	SYNCHRONOUS SEQUENTIAL LOGIC	0	6	12	1	0	0	18	1	19
Unit 3	COMPUTER FUNDAMENTALS	0	11	0	0	0	0	11	0	11
Unit 4	PROCESSOR	0	9	0	0	0	0	9	0	9
Unit 5	MEMORY AND I/O	0	9	0	0	0	0	9	0	9
Total		0	42	32	1	0	0	74	2	75
Total Percentage		0	56	42.7	1.333333	0	0	98.67	2.666666667	100

CO PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	**3**	**2**	**1**	**1**	**2**	**-**	**-**	**-**	**1**	**1**	**2**	1	2	2	1
CO2	**2**	**2**	**1**	**2**	**2**	**-**	**-**	**-**	**1**	**1**	**1**	2	2	2	2
CO3	**2**	**1**	**-**	**1**	**1**	**-**	**-**	**-**	**2**	**1**	**1**	2	2	3	1
CO4	**2**	**2**	**1**	**2**	**2**	**1**	**1**	**-**	**1**	**2**	**1**	3	2	2	3
CO5	**3**	**2**	**2**	**1**	**2**	**-**	**-**	**-**	**1**	**1**	**2**	2	3	3	2
Avg	**2**	**2**	**1**	**1**	**2**	**1**	**1**	**-**	**1**	**1**	**1**	2	2	2	2

Justification for CO-PO mapping

CO1	PO1(3) Graduates will learn the basic knowledge of Boolean theorems,PO2(2) Graduates will able to analyze the k-map in the combinational circuits,PO12(1),Graduates will be able to upgrades their knowledge in design of digital circuits by life long learning
CO2	PO1(2) Graduates will be learn the concept of synchronous sequential circuits,PO3(1) Graduates will able to analyze the design of counters and registers ,PO5(2),Graduates will be able to use modern tools usage in Verilog HDL.
CO3	PO3(1) Graduates will be able identify the architedctures in computer , PO9(2) Graduates will able to slightly gain the contextual knowledge.PO11(2) Graduates will be able to demonstarte knowledge between high level and assembly level language program.
CO4	PO4(2) Graduates will be able analyse the processor.PO6(1) Graduates will be able to understand the contextual knowledge in control unit.
CO5	PO2(2) Graduates will be able to formulate the memory and their hierarchy . PO7(1) Graduates will able to know the need of memory management in a processor..PO12(1) Graduates will be able to learn interconnection standards by life long learning.

3	**High level**	**2**	**Moderate level**	**1**	**Low level**

Name & Sign of Faculty Incharge :Jayanthi.E & Mrs.S.Anusuya

Name & Sign of Subject Expert	:
Head of the Department	:

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