MOHAMED SATHAK A J COLLEGE OF ENGINEERING

Siruseri IT park, OMR, Chennai - 603103

LESSON PLAN

Department of CSE & IT

Name of the Subject	Computer Architecture	Name of the	S. Muthukumar
Subject Code	CS8491	Year / Sem	II/IV
Acad Year	2021-22	Batch	2020

Course Objective

To learn the basic structure and operations of a computer

To learn and implement the arithmetic and logic operations of fixed-point and floating point values

To learn the basics of pipelined execution.

To understand parallelism and multi-core processors.

To understand the memory hierarchies, cache memories and virtual memories.

To learn the different ways of communication with I/O devices

Course Outcome

Describe the basics structure of computers, operations and instructions.

Explain the functions of arithmetic and logic unit.

Understand pipelined execution and various hazards

Analyze the various memory systems and I/O communication.

Explain the parallel processing architectures

Lesson Plan

Sl. No.	Topic(s)	T / R* Book	Periods Required	Mode of Teaching (BB / PPT / NPTEL /	Blooms Level (L1-L6)	CO	PO
UNIT I BASIC STRUCTURE OF A COMPUTER SYSTEM							
1	Functional Units	T	1	PPT	L2	1	PO1, PO2 & PO3
2	Basic Operational Concepts	T	1	PPT	L2	1	PO1, PO2 & PO3
3	Performance	T	1	PPT	L1, L2	1	PO1, PO2 & PO3
4	Instructions: Language of the Computer	T	1	PPT	L2	1	PO1, PO2 & PO3
5	Operations, Operands	T	1	PPT	L1, L2	1,2	PO1, PO2 & PO3
6	Instruction representation	T	1	PPT	L2	1,2	PO1, PO2 & PO3
7	Logical operations	T	1	PPT	L2	1,2	PO1, PO2 & PO3
8	Decision making	T	1	PPT	L2	1,2	PO1, PO2 & PO3
9	MIPS Addressing	T	1	PPT	L1, L2	1,2	PO1, PO2 & PO3
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Quiz							
Evaluation method : Test							
UNIT II ARITHMETIC FOR COMPUTERS							
10	Addition and Subtraction	T	1	BB	L2	2	PO1, PO2 & PO3
11	Multiplication	T	2	BB	L2	2	PO1, PO2 & PO3
12	Division	T	2	BB	L2	2	PO1, PO2 & PO3
13	Floating Point Representation	T	1	BB	L2	2	PO1, PO2 & PO3
14	Floating Point Operations	T	2	BB	L2	2	PO1, PO2 & PO3
15	Subword Parallelism	T	1	BB	L1, L2	2	PO1, PO2 & PO3
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Assignment							
Evaluation method : Mark based							
UNIT III - PROCESSOR AND CONTROL UNIT							
16	A Basic MIPS implementation	T	1	PPT	L2	3	PO1, PO2 & PO3
17	Building a Datapath	T	1	PPT	L2	3	PO1, PO2 & PO3
18	Control Implementation Scheme	T	1	PPT	L2	3	PO1, PO2 & PO3
19	Pipelining	T	1	PPT	L1, L2	3	PO1, PO2 & PO3
20	Pipelined datapath and control	T	2	PPT	L2	3	PO1, PO2 & PO3
21	Handling Data Hazards & Control Hazards	T	2	PPT	L4	3	PO1, PO2 & PO3
22	Exceptions.	T	1	PPT	L1, L2	3	PO1, PO2 & PO3
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Quiz							
Evaluation method : Test							
UNIT IV PARALLELISIM							
23	Parallel processing challenges	T	1	PPT	L2	4	PO1, PO2 & PO3
24	Flynn‘s classification	T	1	PPT	L1, L2	4	PO1, PO2 & PO3
25	SISD, MIMD, SIMD, SPMD, and Vector	T	2	PPT	L4	4	PO1, PO2 & PO3
26	Hardware multithreading	T	1	PPT	L1, L2	4	PO1, PO2 & PO3
27	Multi-core processors and other Shared Memory	T	2	PPT	L2	4	PO1, PO2 & PO3
28	Introduction to Graphics Processing Units, Clusters,	T	1	PPT	L2	4	PO1, PO2 & PO3
29	Scale Computers and other Message-Passing	T	1	PPT	L2	4	PO1, PO2 & PO3
Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any : Role Play							
Evaluation method : Marks based on their presentation and points							

UNIT V MEMORY & I/O SYSTEMS							
30	Memory Hierarchy, memory technologies	T	1	PPT	L2	5	PO1, PO2 & PO3
31	Cache memory – measuring and improving cache	T	1	PPT	L2	5	PO1, PO2 & PO3
32	Virtual memory, TLB's	T	1	PPT	L2	5	PO1, PO2 & PO3
33	Accessing I/O Devices	T	1	PPT	L2	5	PO1, PO2 & PO3
34	Interrupts	T	1	PPT	L2	5	PO1, PO2 & PO3
35	Direct Memory Access	T	1	PPT	L1, L2	5	PO1, PO2 & PO3
36	Bus structure – Bus operation	T	1	PPT	L2	5	PO1, PO2 & PO3
37	Arbitration	T	1	PPT	L2	5	PO1, PO2 & PO3
38	Interface circuits - USB.	T	1	PPT	L1, L2	5	PO1, PO2 & PO3

Suggested Activity: Assignment / Case Studies / Tuorials/ Quiz / Mini Projects / Model Developed/others Planned if any: Assignment

Evaluation method : Marks based

Content Beyond the Syllabus Planned

1	Hardwired programmed control
2	Micro programmed control

Text Books

1	David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Morgan Kaufmann / Elsevier, 2014.
2	Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian, Computer Organization and Embedded Systems, Sixth Edition, Tata McGraw Hill, 2012.

Reference Books

1	William Stallings, Computer Organization and Architecture – Designing for Performance, Eighth Edition, Pearson Education, 2010.
2	John P. Hayes, Computer Architecture and Organization, Third Edition, Tata McGraw Hill, 2012.
3	John L. Hennessey and David A. Patterson, Computer Architecture – A Quantitative Approachl, Morgan Kaufmann / Elsevier Publishers, Fifth Edition, 2012.

Website / URL References

1	**https://nptel.ac.in**
2	

Blooms Level

Level 1 (L1) : Remembering **Level 2 (L2) : Understanding** **Level 3 (L3) : Applying**	Lower Order Thinking	Fixed Hour Exams	**Level 4 (L4) : Analysing** **Level 5 (L5) : Evaluating** **Level 6 (L6) : Creating**		Higher Order Thinking	Projects / Mini Projects

Mapping syllabus with Bloom's Taxonomy LOT and HOT

Unit No	Unit Name	L1	L2	L3	L4	L5	L6	LOT	HOT	Total
Unit 1	BASIC STRUCTURE OF A	3	9	0	0	0	0	12	0	12
Unit 2	ARITHMETIC FOR COMPUTERS	0	9	**0**	**0**	**0**	**0**	9	0	9
Unit 3	PROCESSOR AND CONTROL UNIT	1	8	**0**	**1**	**0**	**0**	9	1	10
Unit 4	PARALLELISIM	2	8	**0**	**1**	**0**	**0**	10	1	11
Unit 5	MEMORY & I/O SYSTEMS	2	9	**0**	**0**	**0**	**0**	11	0	11
Total		8	43	0	2	0	0	51	2	53
Total Percentage		15.09	81.13	0.00	3.77	0.00	0.00	96.23	3.77	100.00

CO PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	**2**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	2	1
CO2	**2**	**2**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	2	1
CO3	**2**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	2	1
CO4	**2**	**2**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	2	1
CO5	**1**	**1**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	2	1
Avg	**1.8**	**1.4**	**1.2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**2**	**1**

Justification for CO-PO mapping

CO1	**Basic Knowledge of structure and Operational Concepts of computer will be gained by students (Engg.Knowledge, Maths)**
CO2	**Knowledge of Arithmetic operations (Mathematics)**
CO3	**Fundamentals of Pipelining concepts(Engg.Knowledge)**
CO4	**Memory and IO systems (Engg. Science)**
CO5	**Parallel processing challenges (Design solutions for Complex engg problems)**

3	**High level**	2	**Moderate level**	1	Low level

Name & Sign of Faculty Incharge : S. Muthukumar

Name & Sign of Subject Expert :

Head of the Department :